



Performance Enhancement of Optimized Dynamic Circuit for Low-Power and High-Speed Applications

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Abstract : In this work the design of a high-speed, low-power dynamic comparator for analog-to-digital converter (ADC) applications is proposed and analyzed. The design incorporates a differential amplifier-based pre-amplifier and a regenerative latch made up the two-stage design of the proposed circuit. In order to improve performance, more transistors are added to act as control switches, isolating the pre-amplifier stage once the latch is engaged. Without compromising comparison accuracy, this method significantly lowers kickback noise and dynamic power dissipation. To achieve a power-delay trade-off, an improved version of the proposed design is also developed, offering flexibility for various design objectives. The Cadence Virtuoso tool is used to construct and simulate the comparator in 45nm CMOS technology. The proposed circuits key parameters such as the power consumption, offset voltage, propagation delay, and power-delay product and offset voltage for which the simulation results are significantly superior to those of conventional dynamic comparators. Because of its enhanced speed and energy efficiency, the recommended comparator is perfect for high-performance, battery-operated, low-voltage ADC systems.

Keywords: Dynamic Comparator, Power-Delay Product (PDP), Kickback Noise, CMOS Technology, High speed ADC, Low Power Design

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1 Introduction

With the growing and rapidly increasing demand of the emerging battery-operated and portable electronics, low-power and high-speed ADCs have become a critical component in many IC system designs in recent years. The comparator, as the key building block in ADC design, largely determines the system performance in terms of overall conversion accuracy, latency, and power efficiency. Further enabled by the severe issues in deteriorating supply voltage, blooming leakage, and uncontrollability brought by the scaling trend of the CMOS technology, comparator optimization has attracted tremendous attention in these days for achieving a high-performance mixed-signal system. Traditional static comparators exhibit a large static power consumption while operating at a lower space overhead due to the required constant biasing and feedback stabilization. To overcome these limitations, dynamic comparators that only consume power during the clock transition have been developed, resulting in 0% static power consumption faster response times.

A typical dynamic comparator consists of a preamplifier and a latch stage. While the latch uses positive feedback to swiftly perform regenerative comparison, the preamplifier shields it from kickback noise and amplifies the small differential input signal. However, older systems still have significant issues with high dynamic power consumption and a long regeneration time, especially at lower supply voltages. draw static current, which causes a significant power loss. To address these problems, recent research has focused on dual-tail dynamic comparators and redesigned latch topologies that increase power efficiency and reduce latency. Previous studies [1]–[3] have shown that timing or switching techniques can be employed to control the preamplifier and latch operation, minimizing unnecessary current consumption and speeding up the comparator. The architecture presented in [4] laid the foundation for future developments by demonstrating a high-speed, high-precision dynamic comparator with short latency, reduced offset voltage, and enhanced preamplifier gain. This study presents, constructs, and simulates an enhanced dynamic comparator in 45 nm CMOS technology using Cadence Virtuoso. The circuit consists of a regenerative latch and a differential amplifier-based preamplifier, both of which are of a two-stage configuration. More PMOS and NMOS transistors are added to both stages so that they act like switches in a controlled manner. As soon as

the latch starts comparing, the preamplifier is disconnected, which reduces kickback noise, dynamic power dissipation, and maintains accuracy in the circuit. Moreover, an optimized version of this circuit is available with fewer transistors, resulting in better power delay product and lower latency, providing designers with more freedom to select between low power and high speed. Unlike conventional two-stage and three-stage dynamic comparators, the proposed architecture employs clock-controlled isolation switches that disconnect the preamplifier once regeneration starts. This reduces unnecessary power dissipation and kickback noise while improving regeneration speed. The inclusion of a double-tail latch and output buffering further enhances speed and stability at low supply voltage.

2 Conventional Comparator

The preamplifier stage and the latch stage are the two primary components of a traditional dynamic comparator. The schematic depicted in Fig. 1 allows for high-speed and low-offset operation. Fig. 1 shows the connections between these stages. Transistors M1–M5 are used in the preamplifier stage, which amplifies the differential input voltage. Here, (V_{in+} , V_{in-}) represent the positive and negative differential input voltages applied to the comparator. and lowers kickback noise coming from the latch stage. While transistors M3 and M4 form the differential input pair, transistors M1 and M2 function as current sink devices that are controlled by the clock signal (CLK). Transistor M5 serves as a clock-controlled current source that turns off the preamplifier during the reset phase and turns it on during the evaluation phase in order to reduce static power consumption.

Transistors M6–M13, which carry out the regenerative comparison, make up the latch stage. Depending on the polarity of the amplified input differential voltage, the cross-coupled inverters made up of M6–M9 create a positive-feedback loop that quickly drives one output node to VDD and the other to ground. Tail transistors M12 and M13 supply the output nodes with discharge paths during the reset phase, guaranteeing a correct initial condition prior to the subsequent comparison cycle.

The pre-amplifier is turned off and the output nodes ($Out+$, $Out-$) are precharged to VDD when $CLK=1$ (reset phase). The evaluation phase starts when CLK changes to 0. The pre-amplifier is activated to amplify the input difference when transistor M5 is turned on. Latch will regenerate that small differential voltage into a full logic level output. This architecture's high speed, low offset, and reduced kickback noise make it especially useful for high frequency applications such as analog-to-digital converters.

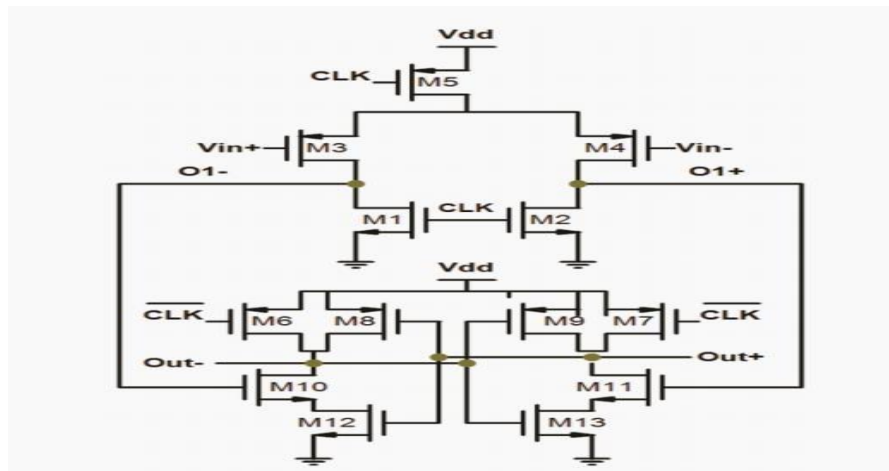


Fig 1 : Conventional Two- Stage Dynamic Comparator

3 Three-Stage Comparator

As shown in Figure 2, the three-stage dynamic comparator consists of a preamplifier stage, an intermediate gain stage, and a regenerative latch stage to provide both fast speed and low power dissipation. By buffering the input from the latch and amplifying the small differential input signals, the preamplifier reduces kickback noise. The preamplifier is formed by transistors M11 and M12. The intermediate gain stage (M13 and M14) amplifies signals QP and QN even further by increasing the voltage difference to ensure that the latch stage receives a large enough differential signal for faster and more accurate decision. The last stage is the regenerative latch (M15–M20) which rapidly converts the amplified differential voltage to full-swing digital outputs with cross-coupled inverters with positive feedback. Transistors M17, M18, M19, and M20 precharge the

output nodes OUTP and OUTN to VDD during the reset phase (CLK=High), guaranteeing a clean starting state for the subsequent comparison cycle. These transistors turn off during the evaluation phase (CLK=Low), enabling the gain and preamplifier stages to process the input differential and trigger the latch for quick, precise decision-making. This three-stage structure is appropriate for high-frequency and precision-oriented applications because it increases gain, decreases offset, and strengthens noise immunity.

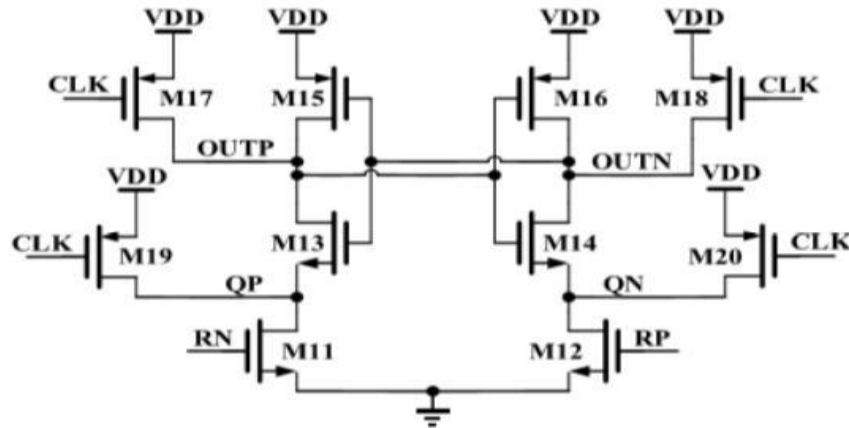


Fig-2 Three- Stage Comparator

4 Optimized Dynamic Comparator

A better dynamic comparator structure is illustrated in Figure 3, which is designed to surpass the traditional and three-stage comparators with regard to speed, power consumption, and offset voltage. To obtain a better performance with regard to noise, a preamplifier, an output buffer, and a regenerative latch are added to the circuit.

Buffer, as well as extra clock-controlled transistors to enhance noise reduction. The preamplifier isolates the input nodes from latch-induced kickback noise while amplifying the input difference moderately. It is made up of clock-driven tail transistors (M1–M2) and differential input pairs (M3–M4, M23–M24). The latch stage (M6–M13) processes this amplified signal by quickly converting the differential voltage at nodes O1+ and O1– into full-swing digital outputs using cross-coupled transistors that provide strong positive feedback. The speed and stability of regeneration are further improved by additional devices (M28, M32). The pre-charge and evaluation stages are managed by the output buffer and control network (M14–M15, M5, M20), which minimizes static power and ensures correct initialization during the reset period. The enhanced comparator achieves lower power by reducing needless node activity and turning off idle stages during reset. improved noise immunity and decreased delay variation. High-performance mixed- signal applications can benefit from the architecture's overall more accurate and efficient comparison mechanism compared to conventional two-stage and three- stage comparators.

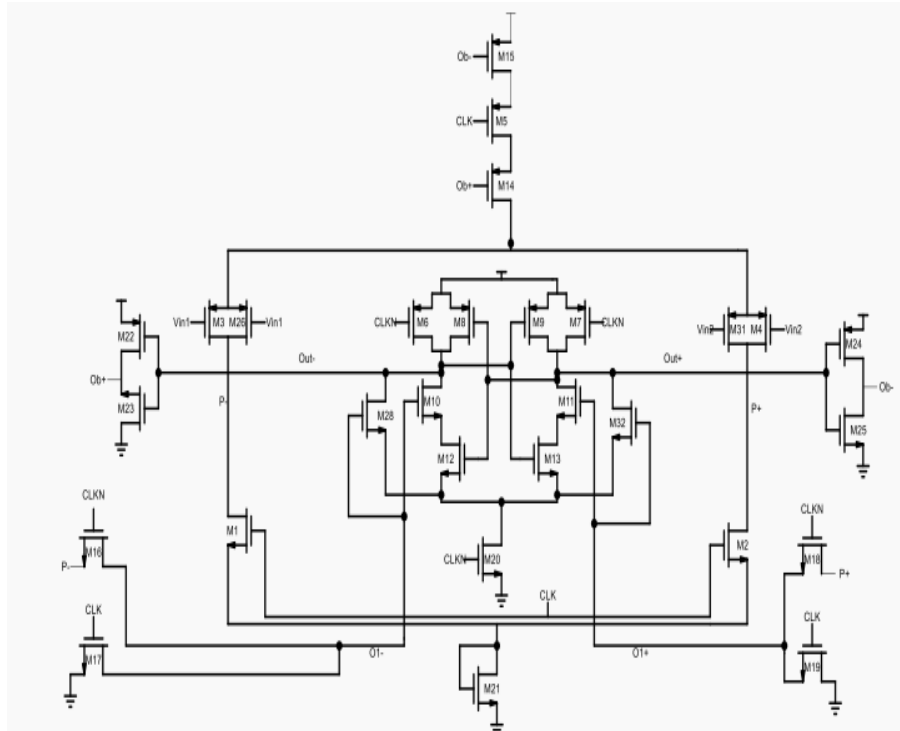


Fig 3: Optimized Dynamic Comparator

5 Proposed Dynamic Comparator

In comparison to traditional two-stage and three-stage comparators, the proposed dynamic comparator design, schematically depicted in Fig. 5, is an improved architecture designed to achieve high-speed operation, reduced power consumption, and superior noise performance. To guarantee precision, the design includes a differential preamplifier stage, a double-tail latch stage, and clock-controlled transistors.

- 5.1 Preamplifier Stage:** The differential preamplifier is what the first stage does. The input transistor pairs linked to IN1 and IN2 isolate the input nodes from significant switching transitions that take place in the latch stage while amplifying the slight input voltage difference. This enhances input sensitivity and significantly lowers kickback noise. At nodes OUT+ and OUT-, the preamplifier transforms the input differential voltage into intermediate differential levels in addition to providing initial gain.
- 5.2 Intermediate Gain and Control Network:** Clock and control nodes (CLK, CLKN, P+, P-) drives several transistors in this design to enhance timing matching and increasing gain. The signal is further amplified by the intermediate network before it arrives at the latch. The pre-amplifier outputs feeds the intermediate network. The static current and total power are reduced since the clock- controlled transistor ensure that each stage is only active during its phase.
- 5.3 Regenerative Latch Stage (Decision-Making Stage):** The double- tail regenerative latch - is the comparator's central component which transforms the tiny, amplified voltage difference into full-swing digital outputs, Strong positive feedback is produced by cross-coupled PMOS and NMOS transistors, allowing for quick regeneration at nodes OUT+ and OUT-. Even in situations with low supply voltage, this configuration increases decision speed and preserves accuracy.
- 5.4 Output Buffer Stage:** The last stage ensures that the output signals (OUT and OUTB) are stable and full swing by acting as an output buffer and driver. In high-frequency applications, it helps sustain high-speed performance and dependable operation by isolating the latch from external load capacitances.
- 5.5 Operating Principle**

Reset Phase (CLK = Low, CLKN = High):

Power is conserved because no current flows in the differential path and all critical nodes are precharged to predetermined levels.

Evaluation Phase (CLK = High, CLKN = Low):

The latch and preamplifier stages turn on. Strong positive feedback is used to first amplify the input voltage difference and then regenerate it into a complete logic- level output.

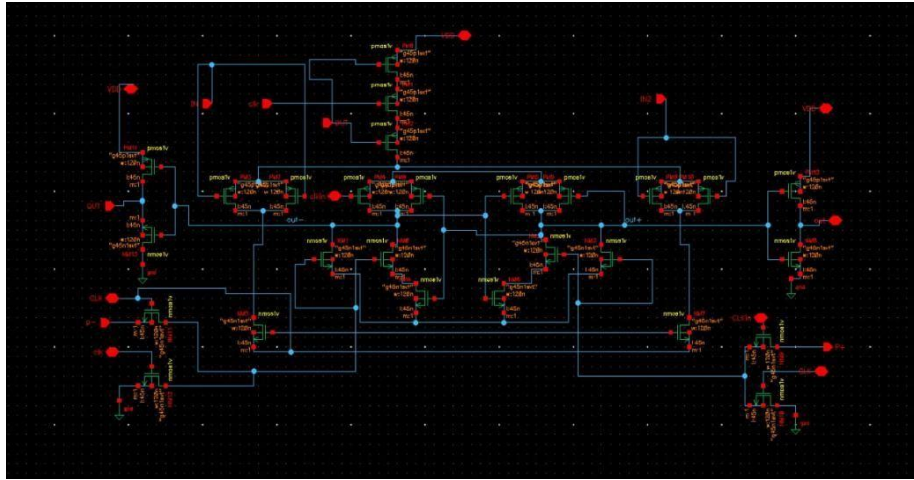


Fig 5: Schematic of the proposed dynamic comparator implemented in 45nm CMOS technology

6 Simulation and Results

The Cadence Virtuoso design environment was used to simulate and implement the suggested dynamic comparator in 45 nm CMOS technology. To guarantee low- power operation, a supply voltage of 0.9 V was employed. To precisely assess switching behavior, transient simulations were run at the proper clock frequency. In order to observe parasitic loading, kickback noise, and regeneration characteristics under realistic conditions, the input drivers and clock generators were incorporated into the testbench.

Correct functional behavior is confirmed by the comparator's transient response, which is displayed in Fig. 6. The differential outputs (V_{out+} and V_{out-}) quickly separate during the evaluation phase, demonstrating strong regeneration and quick decision-making.

During the reset phase, both nodes return to their pre-charged levels, indicating that they have been properly refreshed and are prepared for the subsequent comparison cycle. The synchronous operation of the sampler, Preamplifier, and latch stages is further confirmed by alignment of the input signal, clock transitions, and output levels, guaranteeing stable and dependable comparator performance.

All simulations were carried out at a supply voltage of 0.9 V in 45 nm CMOS technology under identical operating conditions. Monte Carlo mismatch analysis, PVT variations, and layout parasitic extraction are considered as part of future work to further validate robustness.”

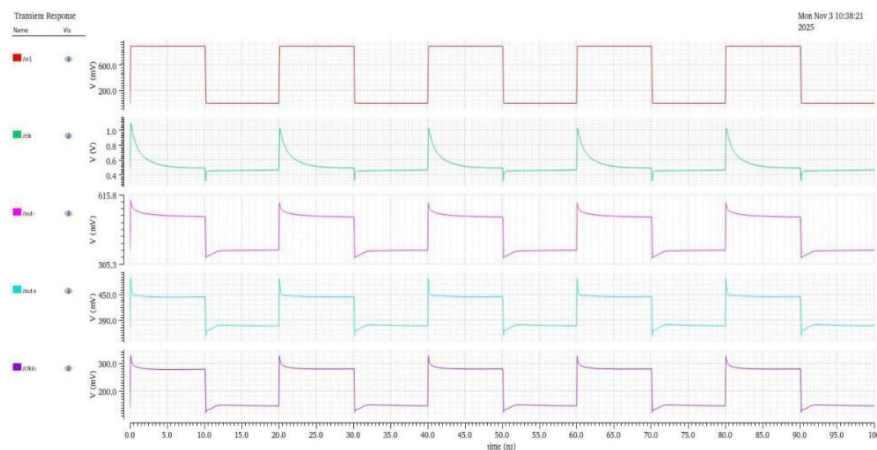


Fig :6 Transient response of the proposed dynamic comparator showing input, clock, and differential output wave forms.

6.1 Power Analysis

The latency of the comparator is typically measured as the period between the clock's rising edge and the moment when the differential output's voltage reaches a valid and observable logic level. This figure is significant because it establishes how quickly the comparator makes a decision. The proposed dynamic comparator has a much lower measured delay than the conventional dynamic comparator has a much shorter measured delay than the traditional dynamic comparator structures, indicating a substantial overall improvement in performance.

This enhancement mainly comes from the latch stage's faster regeneration process and optimized sizing of the input differential pairs, which both contribute to quicker internal voltage difference development. The faster the regenerative nodes split, the quicker the comparison is made and the latch stage has to travel a shorter distance to reach full levels, needing fewer clock cycles. Improved clock-driven switching and smaller parasitic loading also contribute to shorter latency.

In conclusion, the results show that the proposed comparator responds quickly and reliably, making it a suitable option for moderate-speed mixed-signal systems. It performs well in applications that need both speed and accuracy.

6.2 Delay Performance

The latency of a dynamic comparator is a key performance metric that is defined as the time between the rising edge of the clock signal and the point at which the differential output nodes resolve to a stable and distinct logic state.

This delay directly affects mixed-signal systems' overall speed and responsiveness, especially in ADC where fast comparison is required to maintain high throughput and accuracy. The reference data in the comparison table demonstrates that the proposed design's measured delay is significantly less than that of conventional dynamic comparators. An improved regeneration mechanism in the latch stage, which fastens the separation of the output nodes, is responsible for the improvement. Additionally, the optimal sizing and biasing of the input differential pair reduces the initial decision time, enabling a quicker accumulation of the required voltage difference before regeneration.

These improvements make the comparison process much faster. In addition to demonstrating the effectiveness of the proposed architecture, the lower latency highlights its suitability for mixed-signal environments with moderate speeds, where stable decision-making and predictable timing are crucial.

6.3 Power-Delay Product (PDP)

The Power Delay Product (PDP) is one of the significant parameters in evaluating the performance of a high-speed low-power comparator circuit. The proposed comparator has a high value of PDP when compared to most of the existing comparator architectures with a very low value of PDP, i.e., 5.07 fJ. The low decision time along with low power consumption enables a significant reduction in the power consumed during each comparison cycle. This is the major reason for the proposed comparator's high performance. The low value of PDP indicates high energy efficiency, which is a critical requirement for ultra-low power applications like IoT sensor nodes, biomedical front-end circuits, and portable ADC's where every micro-joules of saving can make a big difference in life.

6.4 Offset-Voltage

The input-referred offset voltage of 1.256 mV for the proposed comparator is significantly lower than that of many of the conventional designs mentioned in the table. Offset reduction results from improved charge balance and symmetric regeneration. The low offset ensures higher decision correctness, increased dependability, and increased immunity to input noise. The robust internal reference and good matching of the proposed circuit are confirmed by this small offset value.

The performance metrics, including average power, delay, power-delay product (PDP), and offset voltage, were obtained using cadence virtuoso measuring routines. The delay was calculated using the rising edge of the clock and the differential output decision point. Power was calculated using the average supply current over a continuous clock cycle.

Offset voltage was obtained by employing a differential DC sweep around the common-mode point. A detailed comparison of the proposed design with other comparator designs currently in use is given in Table I. The recommended dynamic comparator has the lowest PDP (5.07 fJ) and power consumption (137.5 nW) of all the designs that were examined. By significantly lowering the propagation latency to 36.9 ns, decision speed is increased while the input-referenced offset (1.256 mV) is maintained low.

These results clearly demonstrate that the proposed design provides the optimal speed, power, and accuracy ratio for low voltage applications.

Table 1. Performance comparison of the proposed Comparator with existing designs

Comparator type	VDD	Power (nW)	Delay (ns)	PDP (fWs)	Offset Voltage (mV)
Conventional Comparator	0.9	977.6	300.34	293.61	1.196
Three Stage Comparator	0.9	237.53	250.12	59.41	4.28
Optimized Dynamic Comparator	0.9	612.20	281.20	171.972	1.2
Proposed Dynamic Comprator	0.9	137.5	36.9	5.07	1.256

All comparator architectures listed in Table 1 are compared under the same supply voltage (0.9 V) and simulation conditions for fair performance evaluation.

7 Conclusion

The paper proposes a high-speed and low-power dynamic comparator using 45nm CMOS technology. In this paper, we propose a novel dynamic comparator that reduces power consumption, enhances the efficiency of regeneration, and minimizes the offset voltage. In this work, we have achieved a very low power delay product of 5.07 fJ with a significantly lower latency of 36.9 ns and reduced power consumption of 137.5nW. In this paper, we have also achieved an offset voltage of 1.256 mV, proving the accuracy and reliability of the proposed design. Therefore, the proposed layout is suitable for low-voltage and low-power mixed-signal applications, including ADCs, biomedical devices, and portable electronics, due to its superior performance compared to other comparator architectures. Long-term temperature variation simulation, Monte Carlo mismatch analysis, and LPE can be considered in future works to validate the reliability of the proposed comparator. In this work, we have achieved a significant improvement in power consumption by approximately 85% and power delay product improvement of approximately 88% compared to the conventional dynamic comparator.

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