

Comparative Analysis of Different Oxides for MoS₂ Transistor

Shivangi Srivastava¹, Md. Ekrama Arshad² and Sajal Agarwal^{1*}

¹Department of Electrical and Electronics Engineering,

Rajiv Gandhi Institute of Petroleum Technology, Jais, Uttar Pradesh, India,

²East Champaran, Bihar, India of Electrical and Electronics Engineering

Rajiv Gandhi Institute of Petroleum and Technology, Amethi, India

¹shivangis1@rgipt.ac.in, ²mdekramaarshad@gmail.com, *sagarwal@rgipt.ac.in

Abstract: The purpose of this study is to evaluate the performance of MoS₂ transistor with different gate oxides. This paper systematically evaluates various performance parameters of transistors such as threshold voltage (V_{th}), on/off ratio, maximum drain current (I_d), transconductance (g_m), and output conductance (g_d). This comprehensive analysis is done using six different oxides namely silicon dioxide (SiO₂), hafnium oxide (HfO₂), lanthanum oxide (La₂O₃), strontium zirconium oxide (SrZrO_x), composite of PMMA:SrZrO_x, and titanium dioxide (TiO₂) for a back-gate device. Results of the paper suggest that SrZrO_x exhibits better performance with lower V_{th} is -0.4 V, along with on/off ratio, maximum I_d , and g_m , are 10^{13} , 662.57 μ A, and 8.12 μ S respectively. Device with a relatively higher on/off ratio, high drive current, high g_m and lower V_{th} demonstrates superior switching and improved performance. With the achieved performance of the above device offers considerable potential for real-time, energy-efficient applications, particularly where power consumption is a big concern. Device with SrZrO_x oxide employed for various real-time applications including wearable electronics, medical and industrial applications.

Keywords: MoS₂, High-k dielectric, gate oxides, Low power applications.

(Article history: Selected papers from NIELIT's International Conference on Communication, Electronics and Digital Technologies (NICE-DT'26), 29-30 Jan, 2026, Gorakhpur, India)

1. Introduction

Molybdenum Disulfide (MoS₂) is an example of TMDC known for its unique properties. Its tunable band gap, ranging from 1.2 eV in bulk form to approximately 1.8 eV in monolayer form, enables efficient light absorption and makes it suitable for a range of optoelectronic applications [1]. Its large area facilitates enhanced charge carrier mobility, leading to improved performance in thin film transistors [2,3]. Furthermore, MoS₂ is the prominent candidate for various applications such as flexible electronics and sensors because of its superior carrier mobility, low leakage current and exceptional chemical stability. However, numerous transistor-based studies have been also reported for wide range of applications [4]. In this sequence, MoS₂ based thin-film transistors (TFTs) are well-established as gas sensors for detecting hazardous gases in real-time [5,6]. MoS₂ based devices also exhibit improved performance, such as high mobility, better on/off ratio, and many more [7]. Thus, it can be summarized that MoS₂ is compatible with different electronic applications and has been used for next-generation devices [8]. Furthermore, performance of MoS₂ based devices is further improved by employing its hybrid structures [9]. Yuning Li et al reported photo-detection capability of graphene/MoS₂ heterojunction-based transistor. The proposed device exhibits excellent photo detection behavior with responsivity $\approx 1.5 \times 10^4$ A/W, detectivity $\approx 3.9 \times 10^{10}$ Jones, and external quantum efficiency $\approx 4.1 \times 10^6$ % [10]. In another study, it is reported that gold (Au) decorated MoS₂ demonstrates superior sensing response as compared to pristine MoS₂ [11].

Choosing high-k dielectric material for gate oxide is another key strategy for enhancing device performance. Employing high-k gate oxide in transistor exhibits superior response of device as compared to silicon dioxide (SiO₂) [12,13]. High-k oxide improves the electrostatic control over gate [14,15], which helps to reduce short-channel effects in scaled devices [16]. As a result, it significantly influences key electrical parameters such as carrier mobility, threshold voltage (V_{th}), and overall functionality of the transistor [17], which contributes to more efficient and reliable transistor operation. Investigating different gate oxide materials for MoS₂ transistors is necessary for improving performance, optimizing interface quality, ensuring scalability, and enabling integration with flexible electronics. It has been investigated that hafnium oxide (HfO₂) exhibits superior device performance in comparison to SiO₂. Device with HfO₂ gate oxide exhibits superior response in terms of various performance parameters including driving current (I_d), oxide capacitance (C_{gg}), on/off ratio, subthreshold swing (SS), V_{th} , and transconductance (g_m) as compared to the device SiO₂ gate oxide. The findings of this study show that device with HfO₂ is suitable for high-speed, power-efficient device, which can be employed for various real-time applications [18]. It is found that both on/off and SS enhances as device's gate oxide switch from aluminum oxide (Al₂O₃) to HfO₂ [19]. It is reported

that utilization of another high-k material i.e., zirconium dioxide (ZrO_2) improves mobility, on/off ratio and SS of MoS_2 device. These values recorded under the influence of ZrO_2 as gate oxide are $89.6 \text{ cm}^2/\text{V}$, 10^8 , and $95.2 \text{ mV}/\text{dec}$ [20]. In another study, a transistor wafer with improved performance is investigated, due to the utilization of ultra-thin high-k HfO_2 as a gate oxide. The above study has relatively low leakage current, low SS, high current density, and on/off ratio i.e., $10^{-6} \text{ A}/\text{cm}^2$, $75 \text{ mV}/\text{dec}$, $260 \text{ }\mu\text{A}/\text{ }\mu\text{m}$, and 10^8 [21]. Thus, it can be concluded that devices with high-k gate oxides are suitable for high-speed, low-power devices. In this study, a comparative analysis is done for MoS_2 transistor for six different dielectrics as shown in Fig.1. The effect of different high-k dielectrics as gate oxide has been visualized through comparing its various aspects, such as on/off ratio, threshold voltage (V_{th}), maximum drain current (I_d), and transconductance (g_m) etc.

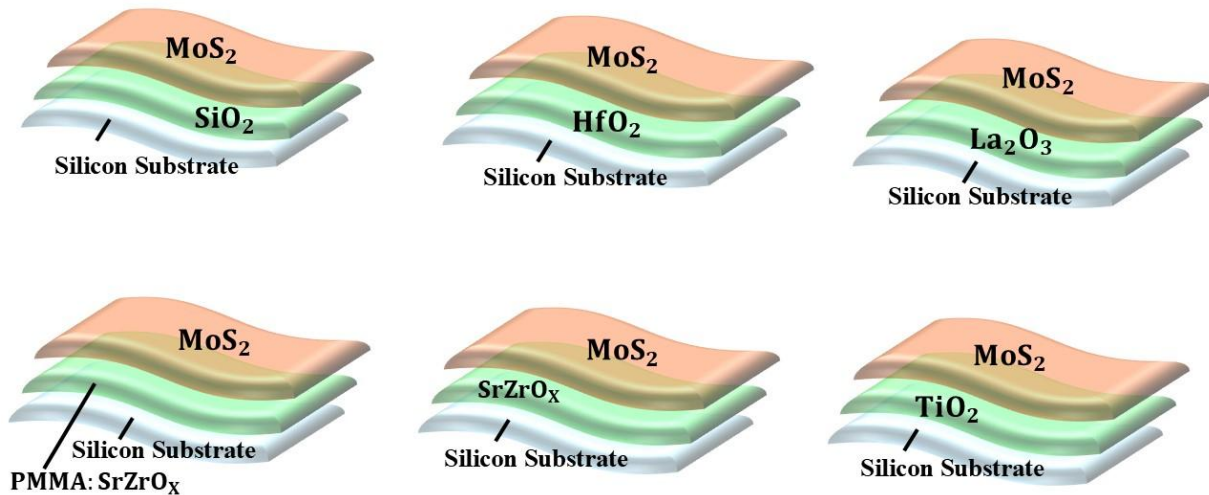


Fig. 1. Transistor geometry with different gate oxide

2. Model Details and Methodology:

Models of the discussed device are simulated by using the semiconductor module of COMSOL Multiphysics 6.4. Dimensions of device used in this study are calibrated in the reported literature by Howell et. al [21]. Furthermore, material properties of MoS_2 are also taken from the ref. [21] and illustrated in Table 1.

Parameters Name	Value	References
Bandgap (eV)	1.6	[21]
Relative permittivity	11	
e^- Mobility ($\text{cm}^2/\text{V} \cdot \text{s}$)	25	
Hole Mobility ($\text{cm}^2/\text{V} \cdot \text{s}$)	25	
Effective mass of holes	$0.5 \cdot m_e$	
Effective mass of e^-	$0.5 \cdot m_e$	

Note: $0.5 \cdot m_e$ is the mass of electron in rest position and it is a constant.

Modelling of the above thin film transistor (TFT) incorporate various numerical equations and models including complete ionization, drift-diffusion mobility modeling, Fermi-Dirac statistics, Poisson's equation, and Shockley–Read–Hall recombination model to establish the accurate simulation of device. In this study, doping of the device with a carrier concentration of $2 \cdot 10^{18} \text{ cm}^{-3}$ represents an intentional and controlled introduction of dopants to achieve specific electrical characteristics. Structure of device is two-dimensional with channel length of device is $3.5 \text{ }\mu\text{m}$. Fig.2 illustrates a comparison of simulated data with experimental data to verify the simulation setup. It has been observed that the experimental data can be reproduced with the help of COMSOL with minute fluctuations, which verify the simulation environment of modelling tool.

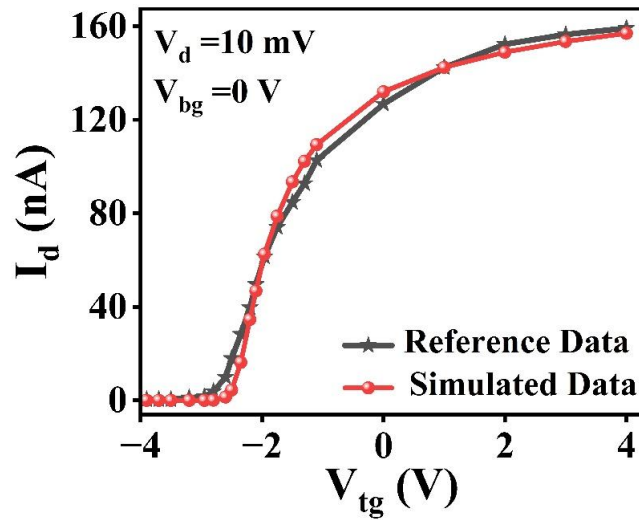


Fig. 2. Calibration of simulation tool with experimental data

Structure of device is shown in Fig. 3, which is tested for different oxides SiO_2 , lanthanum oxide (La_2O_3), HfO_2 , strontium zirconium oxide (SrZrO_x), composite of PMMA: SrZrO_x , and titanium dioxide (TiO_2). Values of dielectric constant of these materials are illustrated in Table 2. All the simulations are performed at room temperature with the same geometrical parameters. These gate oxides with different dielectric constants affect the oxide capacitance of devices which further impact the performance of devices.

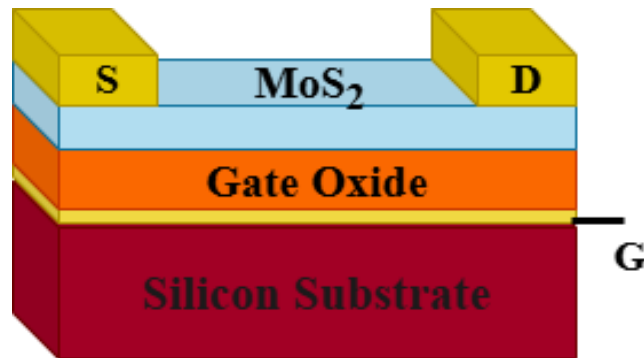


Fig. 3. Structure of MoS_2 transistor with back gate

Table 2: Dielectric constant of used material as a gate oxide

Material	Dielectric constant	Reference
SiO_2	3.9	[22]
HfO_2	20	[23,24]
La_2O_3	27	[25]
SrZrO_x	28	[26]
PMMA: SrZrO_x	32.2	[26]
TiO_2	50	[25]

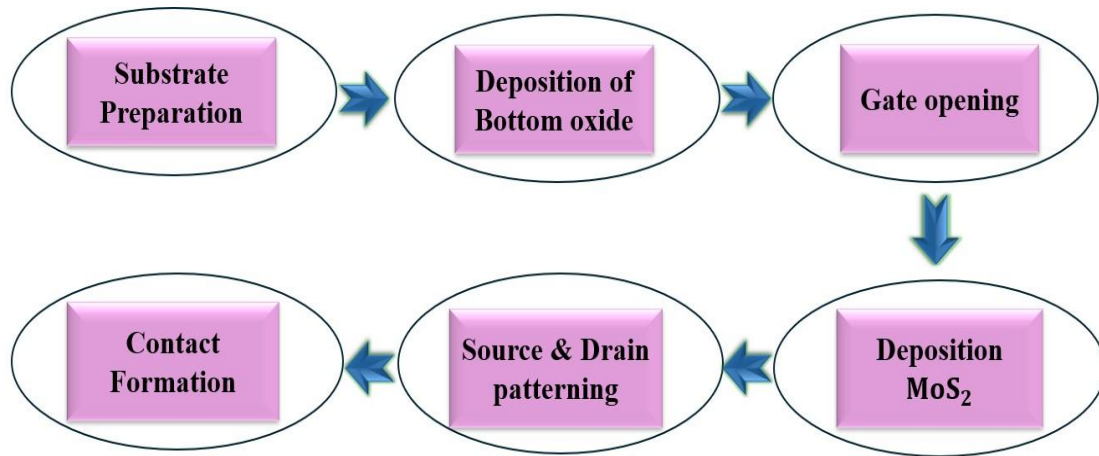


Fig. 4. Possible fabrication steps of proposed device

This simulation study offers various design considerations and detailed insights into the device's performance behavior, which will assist in guiding further device fabrication. Although this is pure simulation study but understanding the feasibility of device, essential fabrication steps are incorporated in Fig.4. The discussed device is the back gate TFT where oxide can be deposited over pre clean silicon substrate. After deposition of oxide, MoS₂ layer can be deposited by one through spin coating. Finally, to facilitate metal contact i.e., source, drain and gate lithography step can be done followed by metallization. Photolithography can be performed using a photoresist and ultraviolet (U.V.) light exposure.

3. Results and Discussion

Performance of a TFT can be analyzed through various electrical parameters such as V_{th} , on/off ratio, maximum I_d , g_m , and g_d etc. The present study is a comprehensive analysis based on the above discussed parameters for different gate oxide including SiO₂, La₂O₃, HfO₂, SrZrO_x, PMMA: SrZrO_x, and TiO₂. Behavior of device has been recorded for these gate oxides, which affects the electrostatic control of the device over the gate and correspondingly leakage current of device changes. Fig.5 shows transfer curve of MoS₂ device for all above discussed gate oxide at $V_d = 0.1$ V. From Fig.5, I_d of device is recorded as 0.74 μ A, 16.63 μ A, 19.83 μ A, 20.20 μ A, 21.21 μ A and 25.24 μ A for SiO₂, HfO₂, La₂O₃, PMMA: SrZrO_x, SrZrO_x, and TiO₂ respectively. V_{th} of device is also extracted from the curve i.e., -4.6 V, -1.1 V, -0.6 V, -0.7 V, -0.4 V, and -0.8 V for SiO₂, HfO₂, La₂O₃, PMMA: SrZrO_x, SrZrO_x, and TiO₂ respectively. For energy efficient and optimum operation of device, lower V_{th} is preferred to reduce power consumption. on/off ratio of the device is extracted from the logarithm of transfer curve and measured as 10^5 , 10^{12} , 10^{12} , 10^{12} , 10^{13} , and 10^{14} for SiO₂, HfO₂, La₂O₃, PMMA: SrZrO_x, SrZrO_x, and TiO₂ respectively. It has been visualized from Fig. 5 that although on/off ratio and I_d of TiO₂ device is better than other oxides, i.e., 10^{14} , and 25.24 μ A respectively, V_{th} associated with TiO₂ is comparatively high. It is also depicted from Fig.5 that SrZrO_x exhibits lowest V_{th} i.e., -0.4 V with relatively comparable on/off ratio. Lower V_{th} indicates the lesser voltage requirement to turn "ON" the transistor, which is an essential parameter for low-power devices whereas higher on/off ratio is mandatory for smooth switching. Thus, it can be summarized that device with SrZrO_x gate oxide demonstrates lower V_{th} with optimum on/off ratio. I_d of device for above discussed gate oxide is further illustrated by Fig. (6). Fig. 6 (a), (b), (c), (d), (e) and (f) illustrated drain characteristics of the device for different oxides, which are essential for knowing the behavior of any device as they establish important parameters, including the voltage drop across the device and maximum achievable drain current. Devices are tested for different values of $V_{gs} = 1$ to 5V with step size of 1 V. Initially, the current increases drastically, indicating a constant increment in the transmission of charge carriers through the channel. However, as the device reaches in saturation, the transmission of charge carriers becomes almost constant due to channel length modulation. From Fig. 6 (a), (b), (c), (d), (e) and (f), it is evident that as the dielectric constant of the device increases, I_d increases. Higher I_d signifies an increment in the electric field due to the accumulation of more charge carriers at lower gate voltage in the channel region. Higher drain current is essential for device performance, as it is an indicative feature of the current driving capability of the device. It has been visualized from Fig. (a)-(f) that I_d of device with SiO₂, HfO₂, La₂O₃, SrZrO_x:PMMA, SrZrO_x, and TiO₂ oxide is 41.9 μ A, 506.79 μ A, 616.84 μ A, 614.32 μ A, 662.57 μ A and 804 μ A respectively. It is also observed from Fig. (a)-(f) that the device with TiO₂ as gate oxide exhibits superior performance in terms of its current drive capability. g_m of the device is a crucial parameter to analyze to evaluate amplification efficiency of transistor. Fig. 7 illustrated variation g_m with respect to V_{gs} of all devices. It is depicted from Fig.7 that device with TiO₂ as gate oxide exhibits superior g_m which signifies its superior amplification capability of signals. Higher drive current of device with TiO₂ gate oxide is responsible for higher g_m of device. It has been

also depicted from Fig.7 that initially g_m start increasing and attain its maximum value. After reaching its peak value at certain voltage g_m starts rolling off which indicates saturation of the device. For the comprehensive analysis of devices, evaluation of g_d of device is mandatory and Fig. 8 illustrates g_d of device for above discussed oxides. It should be minimum for better performance of device. It has been visualized from Fig. 8 that device with TiO_2 oxide exhibits worst g_d whereas SiO_2 shows superior response. Higher I_d associated with TiO_2 oxide device is responsible for lowest g_d . It is also visualized from Fig.8 that g_d of the device for every case g_d decreases for higher value of V_d , which indicates pinch off state of device.

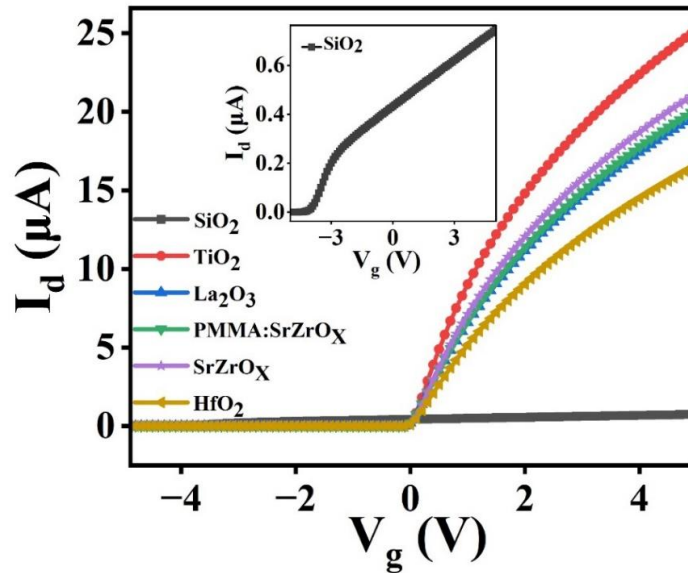
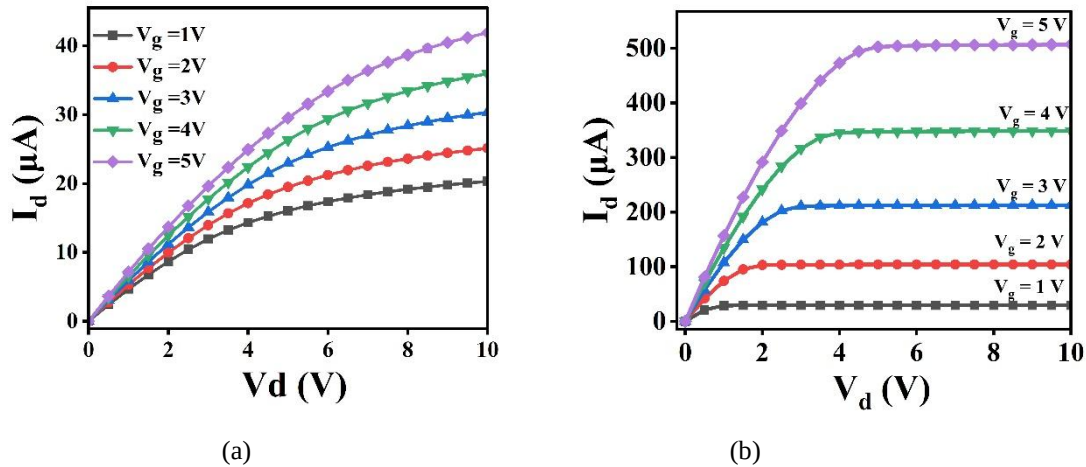


Fig. 5. Transfer curve for MoS_2 transistor at $V_d = 0.1V$ for different gate oxide



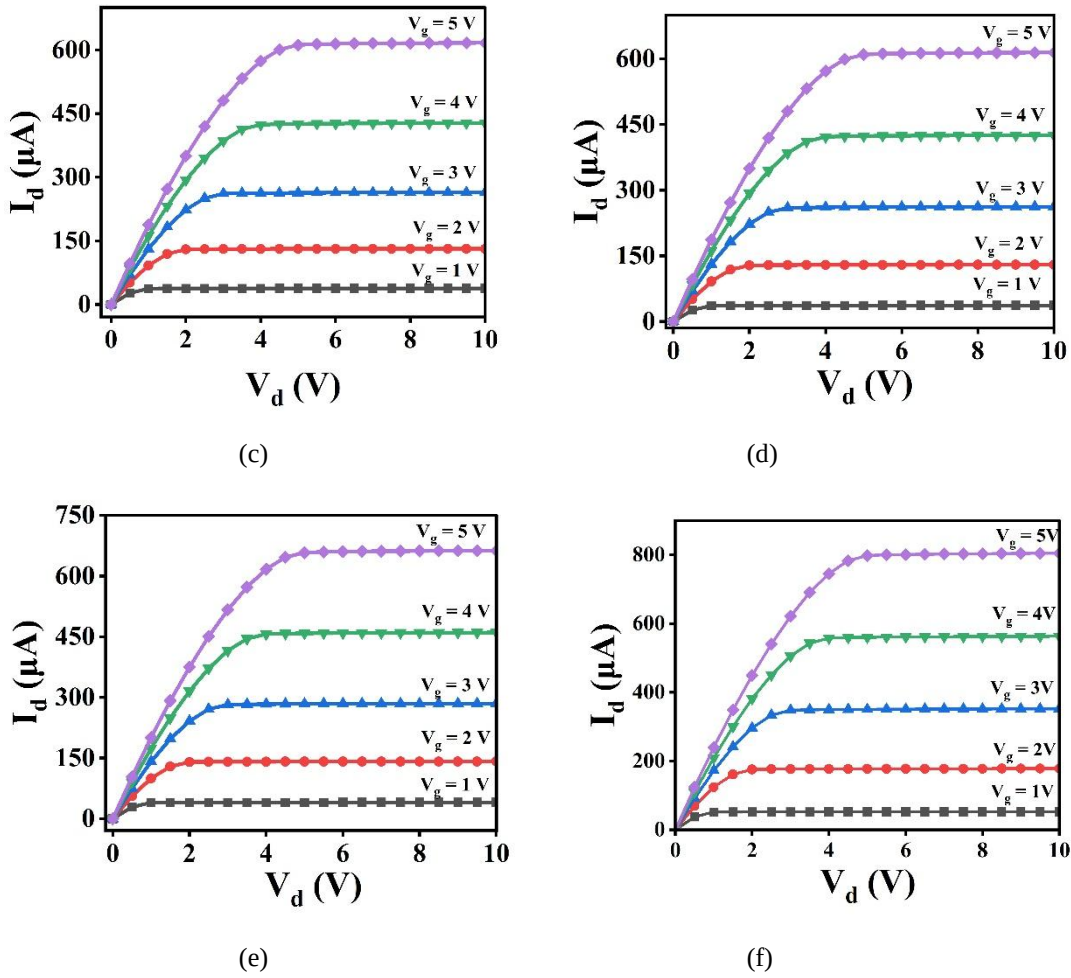


Fig. 6. Output plot for MoS₂ transistor for different gate oxide (a) SiO₂, (b) HfO₂, (c) La₂O₃, and (d) SrZrO_x:PMMA, (e) SrZrO_x, (f) TiO₂

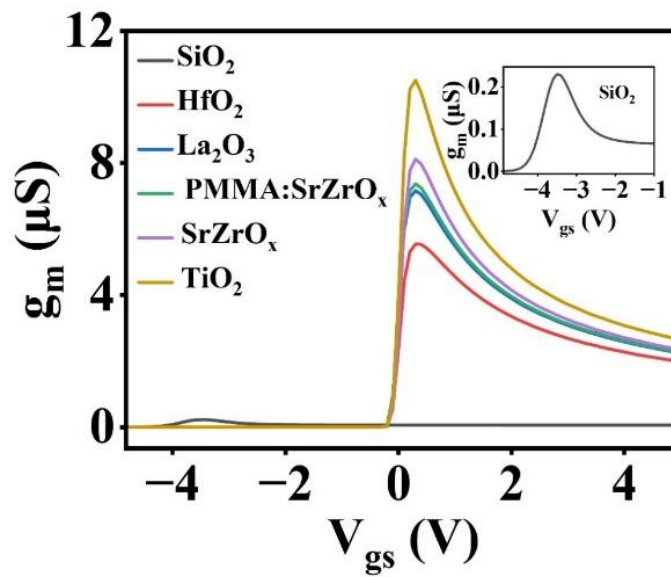


Fig. 7. Transconductance for MoS₂ transistor for different gate oxide

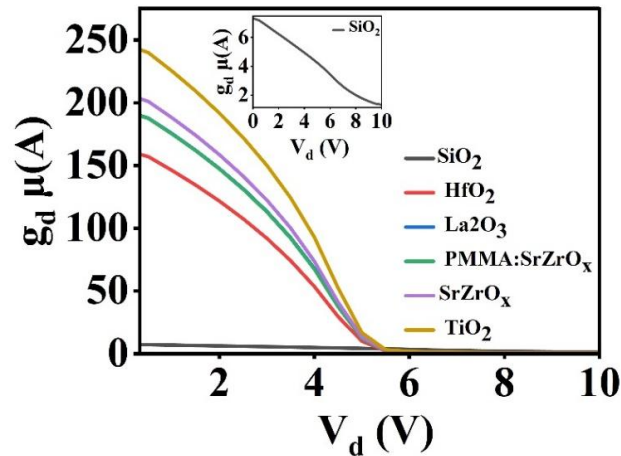


Fig. 8. Variation of output conductance of MoS₂ transistor for different gate oxide

Table 3 illustrates summary of all the performance parameters of MoS₂ transistor for different gate oxides. It has been observed from Table 3 that TiO₂ exhibits highest on/off ratio with highest I_d and g_m , which is 10^{14} 804 μA and 10.51 μS respectively. It has been also analyzed from Table 3 that although TiO₂ has high I_d , g_m and lower g_d , due to relatively higher V_{th} , it can't be used in energy-efficient applications. It is observed from Table 3 that lowest V_{th} is -0.4 V achieved by SrZrO_x with optimum on/off ratio, maximum I_d , and g_m i.e., are 10^{13} , 662.57 μA , and 8.12 μS respectively. Even though TiO₂ has a higher dielectric constant, its higher conductivity and oxygen vacancies lead to charge trapping at the oxide/channel interface, resulting in a relatively higher V_{th} . Thus, it is summarized that the device with SrZrO_x gate oxide exhibits best performance among all the dielectrics used as gate oxides for MoS₂ devices. This device is suitable for low-power circuits or battery-operated applications having lesser V_{th} and moderate on/off ratio and I_d . Device with SrZrO_x gate oxide offers an efficient solution for power hungry equipment such as various battery operated portable appliances and low-power sensors in IoT systems etc.

Table 3. Performance parameters MoS₂ for different oxide

Gate oxide	V_{th}	On/off ratio	Maximum I_d	g_m	g_d
SiO ₂	-4.6 V	10^5	41.9 μA	0.23 μS	7.17 μS
HfO ₂	-1.1 V	10^{12}	506.79 μA	5.55 μS	157.01 μS
La ₂ O ₃	-0.6 V	10^{12}	616.84 μA	7.16 μS	193.768 μS
PMMA:SrZrO _x	-0.7 V	10^{12}	614.32 μA	7.34 μS	193.47 μS
SrZrO _x	-0.4 V	10^{13}	662.57 μA	8.12 μS	201.05 μS
TiO ₂	-0.8 V	10^{14}	804 μA	10.51 μS	239.9 μS

With the above results it can be concluded that only high dielectric constant of gate oxide does not promise its improved performance. For suitable gate oxide bandgap of material also lies in the insulating range. It has been visualized from the results of above study where TiO₂ has highest dielectric constant, but due to its conductive nature limits its performance as a gate oxide. However, device with SrZrO_x as gate oxide exhibits almost comparable performance in terms of drive current along with lowest V_{th} . Fig. 8 (a), (b), (c), and (d) illustrate variation of all the parameters with respect to the gate oxides.

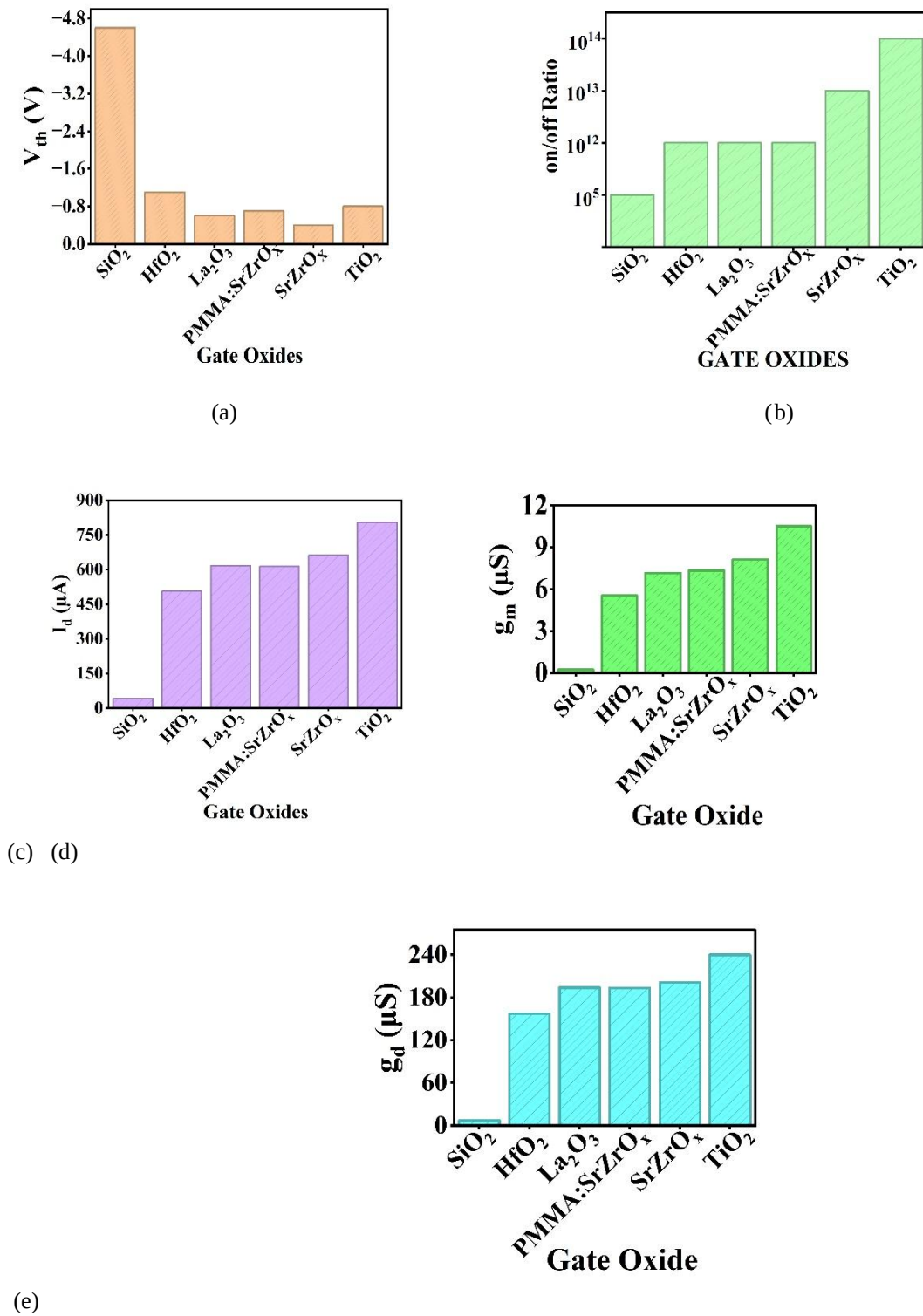


Fig. 9. Variation of electrical parameters with respect to oxides for MoS₂ transistor (a) V_{th} , (b) on/off ratio, (c) I_d , (d) g_m , and (e) g_d

4. Conclusion

The present article evaluates the comparative performance of MoS₂ transistors with different gate oxides. The study highlights that varying dielectric material significantly affects the performance of transistor. From the above study, it is summarized that a material with a higher dielectric constant does not guarantee superior performance of device, as bandgap of the material also plays a significant role. The material used as gate oxide should also have its band gap in the insulator range. Therefore, it is essential to consider all relevant factors before selecting oxide gates to enhance device performance. It can be concluded that although device with TiO₂ oxide demonstrate higher current driving capability, and g_m as compared to other oxides, but it

cannot be useful for low-power device as compared to device with SrZrOx oxide. This device is well-suited for a range of real-time applications, where low-power switching is a big concern. With these performance parameters devices with SrZrOx oxide can be effectively utilized in various fields, including biosensors, digital circuits, and gas sensors, demonstrating its versatility and efficiency across multiple applications.

5. Acknowledgement

Authors would like to express We would like to express gratitude to CST UP for the partial support through the Research Grant "Project ID-3402."

References

1. Singh E., Kim K. S., Yeom G. Y., and Nalwa H. S., "Atomically thin-layered molybdenum disulfide (MoS₂) for bulk-heterojunction solar cells", in "ACS applied materials and interfaces", 2017, vol 9 (4), 3223-3245.
2. Cao W., Kang J., Liu W., and Banerjee, K., "A compact current-voltage model for 2D semiconductor-based field-effect transistors considering interface traps, mobility degradation, and inefficient doping effect", in "IEEE Transactions on Electron Devices", 2014, vol 61 (12), 4282-4290.
3. Srivastava, Shivangi, and Sajal Agrawal, "Potential of nanomaterials in FET-based breath sensing: A comprehensive review & future direction", in "Micro and Nanostructures", 2024, vol 190 207830.
4. Das S., Sebastian A., Pop E. McClellan, C. J. Franklin, A. D. Grasser, & Singh R., "Transistors based on two-dimensional materials for future integrated circuits", in "Nature Electronics", 2021, vol 4, 11, 786-799.
5. Im, H., AlMutairi, A., Kim, S., Sritharan, M., Kim, S., & Yoon, Y., "On MoS₂ thin-film transistor design consideration for a NO₂ gas sensor" in "ACS sensors", 2019, vol 4, 11, 2930-2936.
6. He, Q., Zeng, Z., Yin, Z., Li, H., Wu, S., Huang, X., & Zhang, H., "Fabrication of flexible MoS₂ thin-film transistor arrays for practical gas-sensing applications" in "Small", 2012, vol 8, 19, 2994-2999.
7. Kim, S., Konar, A., Hwang, W. S., Lee, J. H., Lee, J., Yang, J., & Kim, K., "High-mobility and low-power thin-film transistors based on multilayer MoS₂ crystals", in "Nature communications", 2012, vol 3, 1, 1011.
8. Mathew R., and Ajayan J., "Material processing, performance and reliability of MoS₂ field effect transistor (FET) technology-A critical review", in "Materials Science in Semiconductor Processing", 2023, vol 160, 107397.
9. Tsai Y. C., Li, Y., "Impact of doping concentration on electronic properties of transition metal-doped monolayer molybdenum disulfide", in "IEEE Transactions on Electron Devices", 2018, vol 65 (2), 733-738.
10. Li, Y., Sun, J., Zhang, Y., Wang, Y., You, Q., Kong, L., Deng, T., "High-Performance Photodetectors Based on Graphene/MoS₂ Heterojunction FETs", in "IEEE Sensors Journal", 2022, vol 23, 1, 293-299.
11. Chen, W. Y., Yen, C. C., Xue, S., Wang, H., Stanciu, L. A., "Surface functionalization of layered molybdenum disulfide for the selective detection of volatile organic compounds at room temperature", in "ACS applied materials & interfaces", 2019, vol 11, 37, 34135-34143.
12. Wang B., Huang W., Chi L., Al-Hashimi M., Marks T. J., "High-k gate dielectrics for emerging flexible and stretchable electronics", in "Chemical reviews", 2018, vol 118 (11), 5690-5754.
13. Alharbi A., and Shahjerdi D., "Analyzing the effect of high-k dielectric-mediated doping on contact resistance in top-gated monolayer MoS₂ transistors" in "IEEE Transactions on Electron Devices", 2018, vol 65 (10), 4084-4092.
14. Thriveni G., and Ghosh K., "Theoretical analysis and optimization of high-k dielectric layers for designing high-performance and low-power-dissipation nanoscale double-gate MOSFETs" in "Journal of Computational Electronics", 2019, vol 18, 924-940.
15. Salmani-Jelodar M., Ilatikhameneh H., Kim S., Ng K., Sarangapani P., and Klimeck G., "Optimum high-k oxide for the best performance of ultra-scaled double-gate MOSFETs" in "IEEE Transactions on Nanotechnology", 2016, vol 15 (6), 904-910.
16. Narendar V., and Mishra R. A., "Analytical modeling and simulation of multigate FinFET devices and the impact of high-k dielectrics on short channel effects (SCEs)" in "Superlattices and Microstructures", 2015, vol 85, 357-369.
17. Nketia-Yawson B., and Noh Y. Y., "Recent progress on high-capacitance polymer gate dielectrics for flexible low-voltage transistors" in "Advanced Functional Materials", 2018, vol 28 (42), 1802201.
18. Srivastava, S., & Agarwal, S., "Design and analysis of PANI/MoS₂ heterojunction-based transistors for improved analog performance" in "Micro and Nanostructures", 2025, vol 206, 208194.
19. Chang, H. Y., Yang, S., Lee, J., Tao, L., Hwang, W. S., Jena, D., "High-performance, highly bendable MoS₂ transistors with high-k dielectrics for flexible low-power systems" in "ACS nano", 2013, vol 7, 6, 5446-5452.
20. Shi, Y., Liu, G., Wu, X., Zhou, C., Yang, C., Yang, Z., & Shan, F., "UV-Ozone-Assisted Solution-Processed High-k ZrO₂ for MoS₂ Field-Effect Transistors" in "IEEE Transactions on Electron Devices", 2024, vol 71, 4, 2789-2793.
21. Howell S. L., Jariwala D. Wu, C. C. Chen, K. S. Sangwan, V. K. Kang, "Investigation of band-offsets at monolayer-multilayer MoS₂ junctions by scanning photocurrent microscopy" in "Nano letters", 2015, vol 15 (4), 2278-2284.

22. Zhang, L and Li, J and Zhang, XW and Yu, DB and Khizar-ul-Haq, HP Linand Jiang, XY and Zhang, ZL, “Low-voltage-drive and high output current ZnO thin-film transistors with sputtering SiO₂ as gate insulator”, in “Current Applied Physics”, 2010, vol 10(5), 1306-1308.
23. Aldrigo, Martino and Dragoman, Mircea and Iordanescu, Sergiu and Nastase, Florin and Vulpe, Silviu and Dinescu, Adrian and Vasilache, Dan, “Low-voltage permittivity control of coplanar lines based on hafnium oxide ferroelectrics grown on silicon” in “IEEE Access”, 2019, vol 7, 136686-136693.
24. Srivastava S., & Agarwal, S, “First-Principles Investigation of NO₂ Sensing via MoS₂/PANI Heterojunction Transistor” in *IEEE 22nd India Council International Conference (INDICON)*, 2025, (pp. 1-5). IEEE.
25. Mohapatra N. R., Desai M. P., Narendra S. G., and Rao V. R., “The effect of high-k gate dielectrics on deep submicrometer CMOS device and circuit performance” in *IEEE transactions on electron devices*, 2002, vol 49 (5), 826-831.
26. Mehroliya, M. S., Verma, A., and Singh, A. K., “Comparative Analysis of Compact modeled of Low-voltage OTFTs on Flexible and Silicon Substrates for the Implementation of logic Circuits” in *IEEE Journal on Flexible Electronics*, 2024, vol 71(10), 6055 - 6060.