Design and Development of POSIT Arithmetic-Based Digital Beamformer for Ultrasound Imaging System

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Abstract:
Medical ultrasound scanners are among the most advanced signal-processing machines that are presently being used for individual purposes. Over several decades, the operation of ultrasound for medical opinion has been continuously evolving and perfecting. Medical ultrasound, which is also known as individual sonography or ultrasonography, is a safe and effective system fordiagnostic. The beamformer is a critical element of ultrasound scanners, serving as the" brain" that is responsible for the directional transmission and event of the ultrasound signal. Beamforming is a signal processing fashion used in ultrasound imaging to steer and concentrate a ray of sound swells. The work aims to develop a POSIT arithmetic-based digital beamformer for ultrasound imaging systems. The existing ultrasound digital beamformer implementation on hardware is based on either fixed-point arithmetic or IEEE-754 floating-point arithmetic. For fixed-point arithmetic even though the hardware footprint is less it has a problem in achieving a higher dynamic range and in the case of IEEE floating point arithmetic the dynamic range is high but the hardware footprint is larger and more complex. To overcome these drawbacks, it aims to develop a POSIT arithmetic-based digital beamformer for ultrasound imaging systems that have less hardware footprint than fixed-pointand almost the same dynamic range as that of floating-point arithmetic.

Keywords: POSIT Arithmetic, Hardware footprint, Accuracy, Dynamic range, Beampattern

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I. INTRODUCTION

Ultrasound imaging systems are crucial in modern medicine, and their use for medical diagnosis has been advancing for decades. The beamformer is a vital part of ultrasound systems, responsible for forming and directing the ultrasound beam. It plays a critical role in enhancing image quality and diagnostic capabilities. Advances in beamforming technology have greatly contributed to the improvements in ultrasound imaging[1-4].

Ultrasound technology has made significant progress since the 1950s, particularly with the transition from analog to digital beamforming [1]. Previously, analog beamforming was commonly used to steer and focus ultrasound beams. However, it had limitations such as restricted flexibility in beamforming parameters, vulnerability to noise and interference, and challenges in implementing complex imaging algorithms [2][4].

The latest version of the Unum system, known as the type-3 Unum or POSIT format, offers a compromise between the precision of traditional Floating-Point (FP) formats and the efficiency of earlier Unum formats[5-7]. POSITS utilize a unique encoding scheme that allows for a wider range of representable numbers with fewer bits compared to FP formats. They also have well-defined rounding and conversion behavior, addressing some of the issues associated with FP formats. POSITS offer advantages such as larger dynamic range, higher accuracy, better closure, consistent results across systems, simplified hardware, and exception handling. They do not overflow to infinity or underflow to zero, and NaN indicates an action instead of a bit pattern. POSIT processing units require less circuitry compared to IEEE float FPU.

II. LINEAR PHASED ARRAY BEAMFORMING

A linear phased array is a collection of antennas arranged in a line, with each antenna having a different phase shift from its neighbours [8][9]. The block diagram of the linear phased array beamformer is shown in Fig 1. By adjusting the phase shift of each antenna, the antenna array can steer the beam of the transmitted or received signal in a specific direction. This process is known as beamforming. Beamforming using a linear phased array involves adjusting the phase shifts of the

antennas in such a way that the signals from each antenna add up constructively in the desired direction and cancel out destructively in other directions. The delays applied to each element of the array are carefully calculated to ensure that the sound waves emitted from each element are in phase with each other in the desired direction, resulting in constructive interference. This constructive interference results in a focused beam of ultrasound energy that can penetrate deep into the body, improving the image quality and allowing for greater visualization of internal structures. The amount of delay applied to each element of the array is determined by several factors, including the spacing between the elements, the frequency of the ultrasound wave, and the desired direction of the beam. The delay time is usually very small and is typically measured in nanoseconds.The linear phased array is designed with the number of elements as 16 and the sampling frequency is 40MHz.

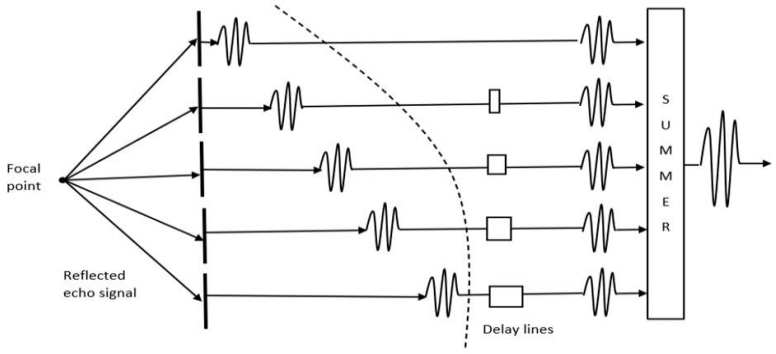

Fig. 1. Block diagram of linear phased array beamformer.

III. Beamformer Architecture

The Beamformer architecture is comprised of four main components: a coarse delay unit, a fine delay unit, an apodization unit, and a summer unit, as illustrated in Fig 2.In the coarse delay unit, a signal is delayed by integer multiples of the sampling period, which can be easily implemented by cascading unit-delay elements. Fine delay, on the other hand, involves delaying a signal by fractional multiples of the sampling period. Apodization is the process of modifying the shape and amplitude of signals by using windowing functions such as Hamming, Hanning, and Kaiser Windows. These functions are utilized to broaden the main lobe and reduce the side lobe amplitude, which helps to reconstruct the signal and mitigate the effects of side lobes. Finally, the summer unit is utilized to combine the signals from the Apodization unit into a single, larger signal. Overall, the Beamformer architecture is an effective means of signal processing that allows for precise control over signal delays and amplitudes.

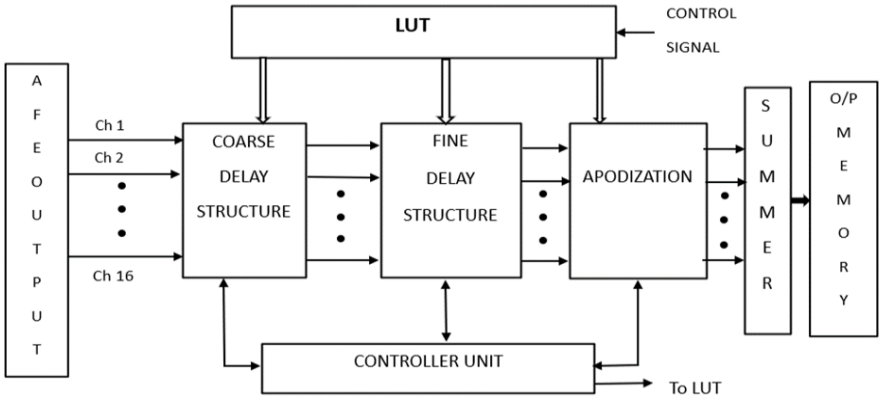

Fig. 2. Block diagram of delay and sum beamformer showing delay elements.

A. Coarse Delay Unit

The block diagram of the coarse delay unit is shown in Fig 3. The coarse delay unit in an ultrasound system consists of FIFO buffers that store input data from the transducer. The data is then fed into D flip flops, triggered by the sampling frequency clock. The output of the flip flops, denoted as Qn, is passed to MUX2. The MUX1 multiplexer selects delay values from Look Up Tables (LUTs) based on scan line angle (Θ) and receive foci (r). The selected delay value determines the appropriate Qn to be chosen and is then sent to the fine delay unit. The LUT stores pre-calculated delay values for the desired scan line angle and receive foci. This process enables the creation of a focused ultrasound beam, allowing for precise control and generation of high-quality ultrasound images.

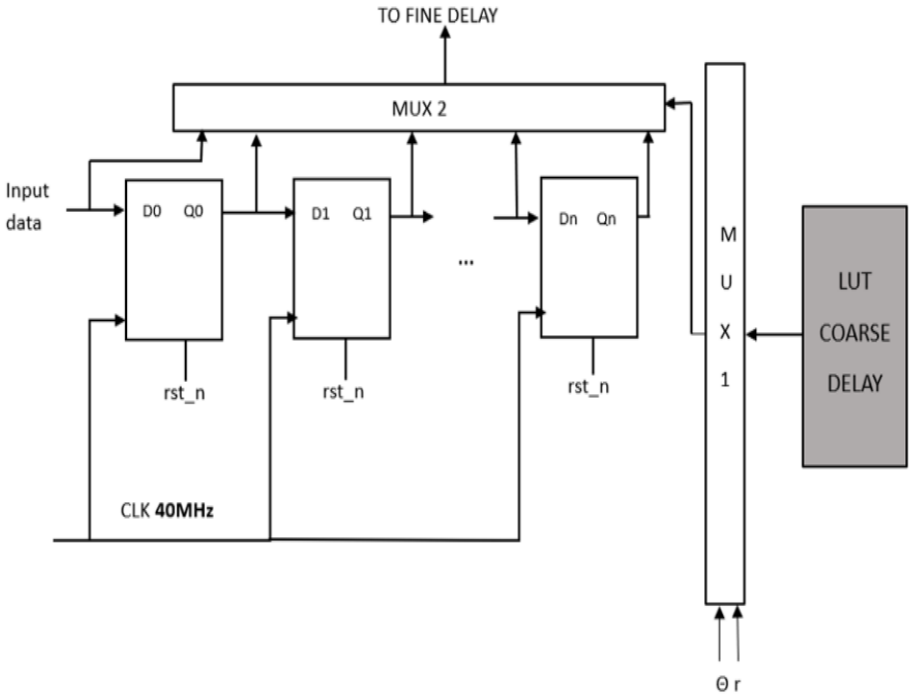

Fig. 3. Block diagram of Coarse delay unit.

B. Fine Delay Unit

The architecture of the fine delay unit is shown in Fig 4. The fine delay unit in the ultrasound system uses a Farrow structure fractional delay finite impulse response (FIR) filter with a minimum mean square error (MMSE) interpolator to adjust the phase of signals by a fractional amount for precise beamforming. The filter coefficients h1 and h2 for the FIR filter are pre-calculated and stored in Look Up Tables (LUTs). The MUX3 and MUX4 select the appropriate coefficients based on the scan line angle (Θ) and receive foci (r) inputs. The Farrow structure employs a D flip-flop with a sampling frequency of 40 MHz. The samples from the coarse delay unit are multiplied by the filter coefficients using a POSIT multiplier, and the results are added together using a POSIT adder. This process ensures that each signal sample is precisely delayed according to the desired beamforming parameters.

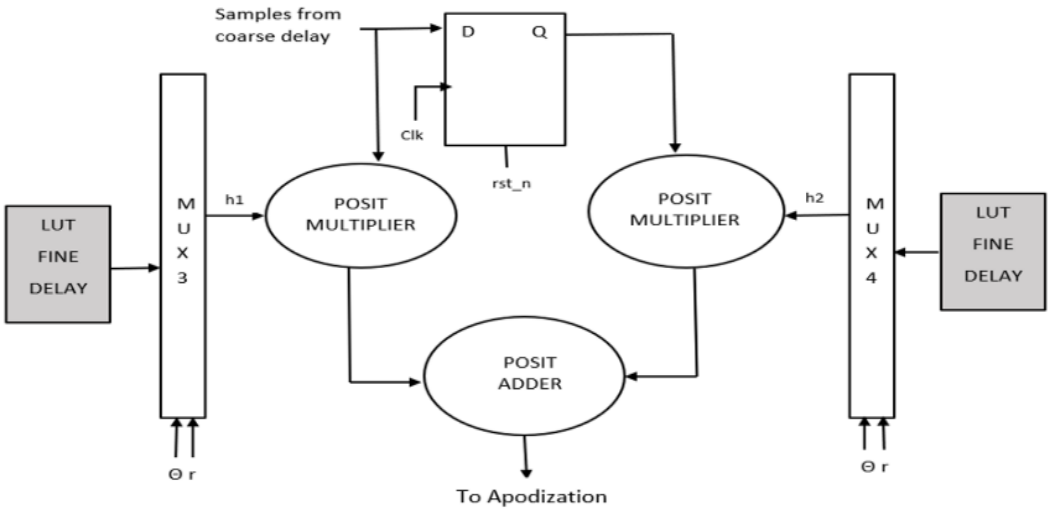

Fig. 4. Block diagram of Fine delay unit.

C. Apodization Unit

Apodization is a signal processing technique applied in ultrasound imaging to enhance image quality by reducing side lobes' amplitude and widening the main lobe of the ultrasound signal. This is accomplished by utilizing windowing functions like Hamming, Hanning, and Kaiser windows, which are employed after the coarse and fine delay stages. The

apodization unit's block diagram, shown in Fig. 5, includes Look Up Tables (LUTs) storing the window functions. The user can choose the desired window function using a parameter called "Apo select," with the Hanning window function being the default choice in the current implementation. During the apodization stage, the signal samples are multiplied by the corresponding window function weights obtained from the LUT using a POSIT multiplier. This multiplication broadens the main lobe of the signal, resulting in improved image resolution.

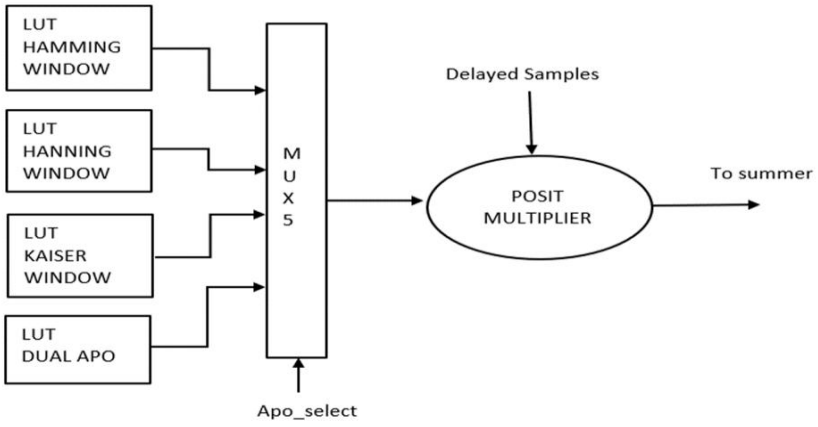

Fig. 5. Block diagram of Apodization unit.

D. Summer Unit

The signals from 16 channels are added together using a POSIT adder. The POSIT adder performs addition on the input signals in POSIT format[10-12].

E. Output Memory

After the beamforming process, the resulting image data is stored in a ping-pong memory. The data is read from one memory bank and processed to produce the final image while the other memory bank is being written to with new beamformed data [13-15]. This allows for the continuous acquisition and processing of ultrasound signals, providing real-time imaging capabilities.

IV. Design

A 16-channel digital beamformer is designed using Vivado IDE and Kintex-7 KC705 evaluation board. Verilog HDL is used to write the source codes for different blocks and components, which are integrated into the top_dbf_16 module using structural Verilog. The design flow involves creating LUTs for window functions using Matlab and Simulink. The main module, top_dbf_16, contains sub-modules for delay, apodization, and delay control. The delay module consists of coarse and fine delay units, responsible for appropriate signal delays [15]. The apodization unit applies window functions to shape the frequency response [13]. POSIT arithmetic is used for multiplication operations in each channel. The resulting signals from all channels are added together using POSIT adders to form the beam. The delay control unit manages and controls the delay modules for accurate beamforming. Each channel has its own delay module, including input memory/FIFO, coarse_delay_unit, and fine_delay_unit. The input data is buffered in the FIFO, and the coarse_delay_unit provides coarse delays based on LUT values. The fine_delay_unit implements fine delays using filter coefficients stored in DPRAMs and performs multiplication and addition operations using POSIT arithmetic. The design ensures synchronized and reliable beamforming by managing input data, applying appropriate delays, and performing accurate calculations. The design flow diagram is shown in Fig 6.

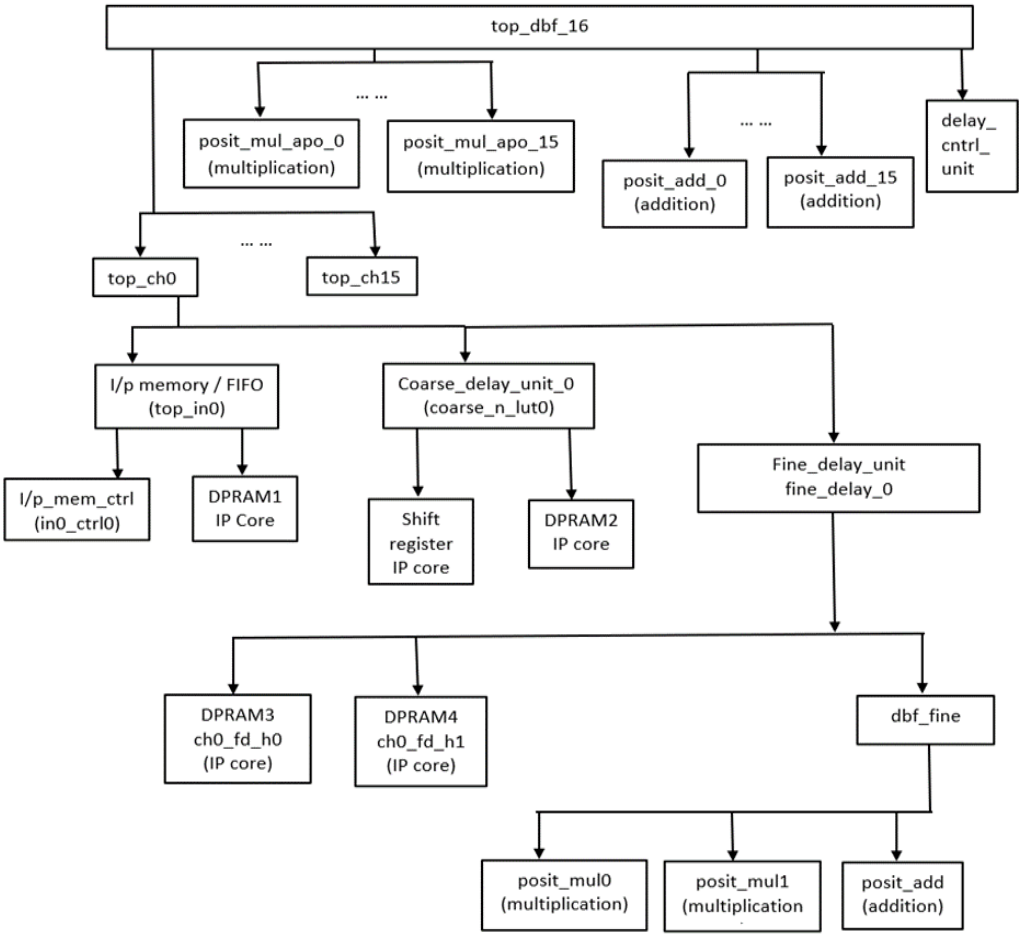

Fig. 6. Design flow diagram of posit arithmetic-based digital beamformer.

V. RESULTS

The digital beamformer is designed using Verilog HDL and utilizes 16-bit POSIT arithmetic. The entire digital beamforming system, which was designed using the 16-bit POSIT arithmetic and Verilog HDL, was implemented on the Xilinx kintex-7 FPGA kc705 evaluation board. To assess the performance of the implemented design, various parameters such as resource utilization, accuracy, and dynamic range were evaluated and compared with those of beamformers utilizing other arithmetic types, such as 64-bit fixed-point beamformers and 16-bit floating-point beamformer.

The beampattern of the 16-bit POSIT arithmetic-based beamformer was analysed and is presented in Fig. 7. This provides a visual representation of the performance of the system and its ability to accurately focus the beam in the desired direction. Here, the beam is steered at an angle of 0°.

The resource utilization of the 16-bit POSIT arithmetic-based digital beamformer was compared with the 64-bit fixed-point beamformer and the 16-bit floating-point beamformer. Table-I and Fig. 8 present a summary of this comparison, highlighting the efficiency of the 16-bit POSIT arithmetic-based beamformer in terms of resource utilization. Notably, the implemented system requires approximately 65% fewer resources than the 16-bit floating-point arithmetic-based architecture.

The accuracy of the 16-bit POSIT arithmetic-based digital beamformer was assessed by evaluating the peak noise or error in the transmitted bit-stream and comparing it with a 32-bit IEEE-754 float MATLAB model. The beamformer was steered at an angle of 0° and the signal was sampled at a rate of 40 MHz. This evaluation included comparisons with digital beamformers using different arithmetic types. The results, illustrated in Fig. 9, indicate that the 16-bit POSIT arithmetic-based beamformer outperforms the 16-bit floating-point and 64-bit fixed-point arithmetic-based beamformers in terms of peak noise or error. This demonstrates the superior accuracy of the 16-bit POSIT arithmetic-based beamformer in comparison to the other arithmetic types [16].

TABLE I. RESOURCE UTILIZATIONCOMPARISON

	16-bit Posit	64-bit Fixed-Point	16-bit Floating-Point
Resource	Utilization (%)	Utilization (%)	Utilization (%)
LUT	4	17	19
FF	1	16	81
IO	51	88	39
BUFG	3	3	3

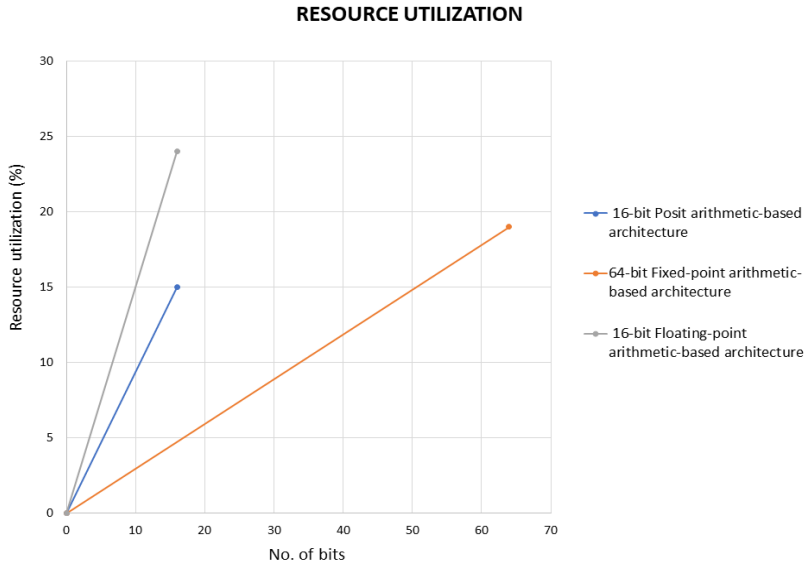

Fig. 8. Resource utilization comparison.

The dynamic range of the 16-bit POSIT arithmetic-based digital beamformer was compared with that of the 16-bit floating-point and 64-bit fixed-point arithmetic-based beamformers. Table-II and Fig. 10 present a summary of the results. It was observed that the dynamic range of the POSIT architecture outperforms the fixed-point architecture. The dynamic range of the 16-bit floating-point and POSIT architectures, on the other hand, was found to be comparable, with higher bit-size floating-point architectures exhibiting greater dynamic range.

VI. CONCLUSION

A 16-bit POSIT arithmetic-based beamformer was created using Verilog HDL and simulated with Xilinx Vivado design suite. Performance matrices were evaluated and compared with 16-bit floating-point and 64-bit fixed-point arithmetic-based beamformers, including resource utilization, accuracy, and dynamic range. The observations indicate that the POSIT arithmetic-based architecture provides greater accuracy and dynamic range while using fewer resources. The resource utilization of the implemented work is fewer than the 16- bit floating-point arithmetic based beamformer by about 65%. The implemented design combines the benefits of both floating-point and fixed-point arithmetic-based beamformers. The POSIT arithmetic-based digital beamformer is a more efficient and cost-effective solution compared to other arithmetic types, making it an excellent replacement.

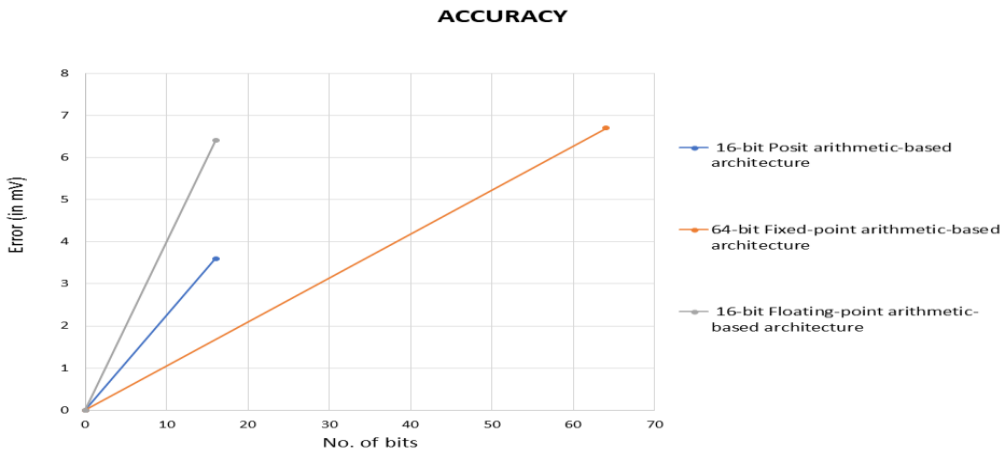

Fig. 9. Accuracy comparison

TABLE II.DYNAMIC RANGE COMPARISON

No. of bits	Fixed-point DR (in dB)	Floating-point DR (in dB)	Posit DR (in dB)
16	96	192	169
32	192	1541	1445
64	385	12330	5973

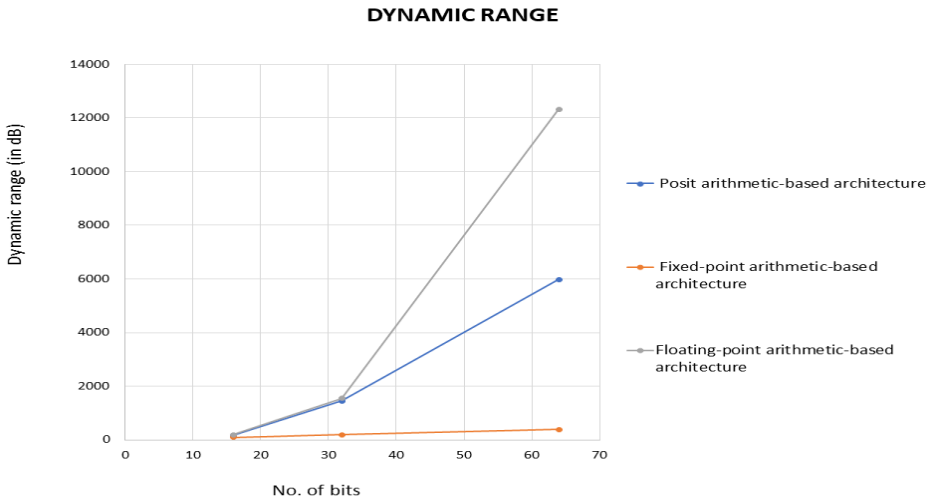

Fig. 10. Dynamic range comparison.

VII. FUTURE SCOPE

The posit algorithm is a relatively new and developing concept that has shown promising results in improving the accuracy and efficiency of computing systems while using fewer bits compared to traditional arithmetic methods such as fixed-point or floating-point arithmetic. The advancements in the posit algorithm offer a promising direction for the development of more accurate and efficient beamformers with reduced resource utilization and fewer bits, which can have significant implications for a wide range of applications, including communication systems, medical imaging, and radar systems.

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