Design and comparative analysis of low power,area efficient optimized 10T Hybridfull adderfor high performance Arithmetic and Logic Unit

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Abstract

In this time of rapid invention and utilisation of battery-operated products, battery life is a significant problem. Because the traditional Full Adder(FA) uses more energy, we used low power FA circuitry in this study and examined how it functions in lieu of the traditional Full Adder circuitry. Contrary to the latest State of Art, only ten transistors make up the suggested design, which runs on a 0.8 supply voltage. This study compares and contrasts the present design with the FA's suggested work in respect of power and delay. This design consumes low power of only 674.38 nWand is area efficient as it consists of only ten transistors. The presented design of FA consumes less power and offers very less delay of only 2.3 ps than existing designs. TANNER EDA is used to simulate proposed FA and using a 65nm CMOS technology.

Keyword: Addition, XOR, XNOR cell, Low power, Full adder (FA) Hybrid design.

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1. INTRODUCTION

Real-time signal processing, including audio, picture, and video processing, has become possible because to recent technological breakthroughs in multimedia and digital communication systems. Subtraction, Multiplication are all types of addition that are used in many applications, includingdigital signal processing & processes like convolution and filtering transformation. The central component in each of these modules [1] is the 1-bit FA cell.Due to the demand for reduced power usage in portable devices like laptops and smartphones. The three most important aspects to consider while designing a VLSI chip for high performance are power consumption, compact area, and fast speed [2-5]. There were other methods for designing VLSI circuits to reduce surface area and power consumption, but one of the best is gate diffusion input method[2]. In order to decrease area, latency and power consumption while still achieving full-swing output, this paper aims to construct a 1-bit FA circuit employing full-swing GDI(Gate Diffusion Input) based FA. A GDI based approach is an efficient technique for designing a 1-bit full adder in VLSI circuits. In this approach, the full adder circuit is designed using a combination of NMOS and PMOS transistors along with gate diffusion inputs. The GDI technique offers advantages such as reduced power

consumption, improved performance, and simplified design. By carefully selecting the transistor sizes and configuring the gate diffusion inputs, the FA circuit can be optimized for area, power, or speed, depending on the application. The proposed GDI based 1-bit FAcan be used in arithmetic logic units (ALUs), Vedic Multiplier, microprocessors, and other digital systems where addition operations are required. It provides a fundamental building block for various computational tasks and plays a crucial role in the overall functionality and performance of VLSI systems.In this paper we analyse the impact of technology scaling on the performance of GDI FAs and highlight the trade-offs associated with each design. The study offers valuable insights into selecting an appropriate GDI-based FA for low-power applications in nanoscale technologies. The structure of this paperis:The GDI approach is described in Section 3., along with its advantages and disadvantages. In Section 4, the FA Cell's design is covered. In Section 5, the applications of the FA Cell's design ispresented. The comparison and simulation results are in Section 6. The paper is concluded in Section 7.

2. EXISTING LITERATURESREVIEW

In [1],the authors present a novel, low-power, energy-aware full-swing FA based on a hybrid logic architecture. A feedback loop, an inverter, and a pass transistor of a 3T gate of XOR-XNOR logic are first combined to create a novel energy-efficient 10T cell of XOR XNOR logic. A novel complete FA circuit is created and tested in 180nm TSMC CMOS process semiconductor technology using the optimized cell and two additional modules after the performance of the recommended cell in this work is compared to that of other research papers. The simulation findings were validated using the Cadence Virtuoso tool, which revealed gains in power usage and power delay product of 33.74 and 35.81 percent, respectively, over earlier studies. Furthermore, simulations of voltage, process, and temperature (VPT) variations are used to substantiate the high-performance promise of the full adder cell in our suggested concept. Finally, it was shown that their unique design has great power dissipation and power dissipation performance by using various complete addersimplementation in four-bit ripple carries adders (RCAs). In order to prevent short circuit power consumption, this study developed a novel adder architecture based on hybrid logic employing circuits and restricted transistors in two modules. Transistors must be positioned appropriately in the layout design, showing that the main factor in low-power performance was the lowering of switching capacitances. A four-bit ripple carry adder is also created to show the recommended architecture's effectiveness for challenging circuits.

In [2], the authors present a design that reduces area, latency and power consumption while giving full swing output for logic 1 and logic 0 for 1-bit FA cells. One 2x1 multiplexer(MUX) cell and two XOR gate cells constitutes entire adder circuit. Using TSMC 65nm technology models on cadence virtuoso simulation at low supply voltage and 125MHz frequency, the performance of the optimised design for full adders was compared with that of numerous logic designs. The simulation results show that the proposed FA architecture outperforms all existing solutions in respect of latency and space while consuming little power.

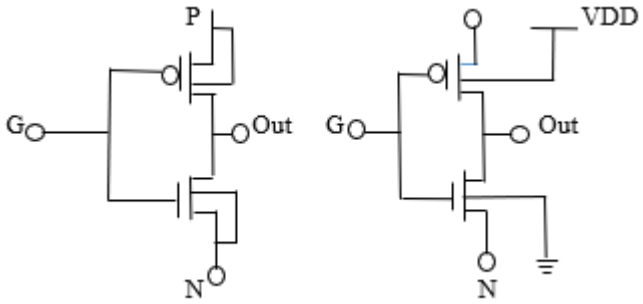
In [3], the authors describe adder cells that use the Gate Diffusion Technique (GDI) and PTL-GDI techniques. The power consumption, propagation delay, and PDP (power delay product) can all be reduced using the GDI technique, whereas the Pass Transistor Logic (PTL) method minimises the number of transistors needed to create various logic gates by removing unnecessary transistors. Performance comparisons between different hybrid adders are shown. Using GDI and PTL approaches, we suggest two new designs in this work that are far more power-efficient than those already in use. The SUM & CARRY function is implemented in both systems using just 10 transistors.In order to implement the SUM and CARRY cells, the XOR cell must first be implemented. The SUM and CARRY cells are then implemented utilising the XOR as an input. The SUM and CARRY cells for the proposed GDI adder were created utilising the GDI method. of contrast, the SUM cell of the proposed PTL-GDI adder is built using PTL approach, while the CARRY cell is built using GDI technology. There is discussion of the benefits of both designs. The simulation results from the Cadence Virtuoso 180nm environment support the relevance of these designs.

In [17], the authors offer a design that is implemented using different types of logic systems, each of which serves a certain purpose in the hybrid system. A hybrid Full Adder cell with a single bit is used in this arrangement. A 16-nm CMOS hybrid full adder is used to research the suggested strategy. The suggested architecture exhibits great efficiency in both power consumption and delay based on the results of the simulation. The simulation's results showed that modern high-speed central processor units included a full adder circuit as part of their data channel

architecture. This kind of hybrid full adder reduces latency while boosting efficiency and is mostly used in nanotechnology applications.The average power consumption of 1.5317 W with a reasonably low latency of 10.4078 n was found to be extraordinarily low for a 1 -V supply in 16-nm technology.

3. GATE DIFFUSSION INPUT(GDI) TECHNIQUE

GDI isan alternative to the CMOS logic design for low power and compact silicon area of VLSI digital architecture, was developed in 2002 [4]. Additionally, it offers a more efficient method for designing quick, low-power devices with fewer transistors than CMOS, Pass Transistor Logic(PTL), and Transmission Gate(TG) methods. In fig.1 (a) Primitive Optimized GDI cellis presented and in fig. 1 (b) Modified GDI Cell is presented.



(a) **(b)**

Fig.1:GDI based Designs [4]

By this method many complex expressions can be designed using only 2 transistorsas mentioned in Table 1.

Table 1: Complex Function using 2 Transistor

N	P	G	OUT	FUNCTION
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A} + B$	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B + AC$	MUX
0	1	A	$\bar{A}$	NOT

This logic type has various drawbacks, namely lower output voltage swing caused by threshold drops, which means the output voltage, whether high or low, deviates from V_{DD} or GND by the threshold voltage drop (V_{th}), degrading performance and boosting short circuit power. In order to solve this issue, modified gate diffusion input logic style (MODGDI) was created [4], which is fundamentally different from the classic GDI cell in that the PMOS and NMOS substrate terminals are connected to V_{DD} and GND, respectively (b).In comparison to the fundamental GDI logic, this logic enhances output Voltage Swing, power, and also power delay product. It is suitable for implementing in a conventional CMOS process. In [5], a novel strategy called as the Full Swing (FS) GDI technology, which relies solely on swing restoration transistors (SR) to guarantee the full swing functioning for the Fl and F2 functions. This strategy aims to increase output swing and solve the threshold drop problem. Any logical function may be realised using either Fl or F2 gates or a mix of the two. Although this method employs additional transistors than conventional GDI, it employs less transistors compared tothe CMOS logic style and provides full swing output, little latency,low power, and compact size of the circuit. In various case studies of various VLSI components, including adders, multipliers, and flip-flops, highlighting the benefits of the GDI approach in terms of power, area, and speed.

4. PROPOSED DESIGN OF FA

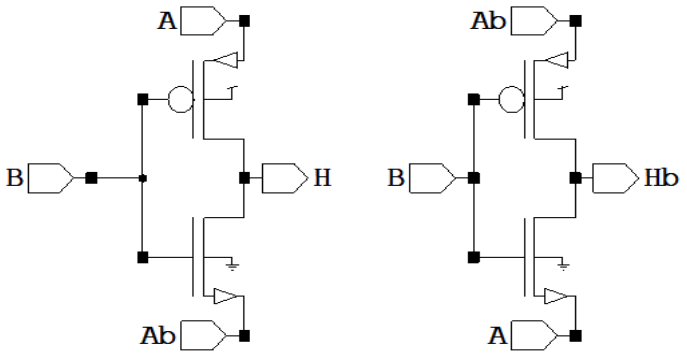
The proposed hybrid FA architecture gains relatively less power and delay. Studies have shown that full adder is designed in less PDP oriented CMOS perform better than the rest of most cells of conventional full adder which perform better by considering various loads on the supply voltage scale. The following circuits are realised in this work using the Full-Swing GDI approach in order to create the FA.

A. XOR & XNOR Gate

A few examples of digital circuits are a comparator, adder, decoder, multiplier and compressors that may be realised using the XOR gate as their fundamental building component [6]. As illustrated in fig. 2, the design of XOR& XNOR gate requires 2 transistors each (a)& (b). When NMOS is turned off at V_{in}—V_{tp}>V_{out}>V_{DD}, then the output of XOR gate becomes equal to the threshold voltage of the PMOS transistor (V_{tp}). In the linear region, V_{in}—V_{th}<V_{out}<V_{DD}, NMOS is switched off at A= 0, followed by PMOS, and the output of XOR equal to V_{DD} subsequently flows through PMOS. When the PMOS transistor is cut off at A=1, V_{in}<V_{out}<V_{DD}, the NMOS transistor is turned on, and then the output of the XOR gate is equal to V_{DD}-V_{th}, the NMOS transistor's (V_{tn}) threshold voltage. When A=l, B =1,then PMOS is turned off, NMOS is in linear region and the output becomes equal to ground then passes through the NMOS. Summary of XOR gate functioning is shown in table II.

Table 2: XOR & XNOR Gate Truth Table

A	B	A ⊕ B	A ⊙ B
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1



(a) (b)

Fig.2: Schematic of (a) 2T XOR GATE [H = A ⊕ B] (b) 2T XNOR GATE [Hb = A ⊙ B]

B. Sum Generator Circuit

The Sum circuit consist of 2T XOR Gate as shown in Fig. 3. It generates Sum (A ⊕ B ⊕ C) by XOR of output of XOR Stage H (A ⊕ B) &bit C_{in}.

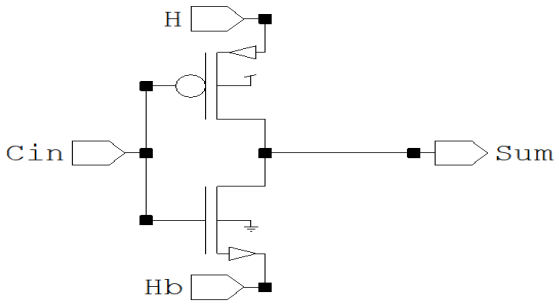


Fig.3: Schematic of Sum Circuit

C.2x1 Multiplexer

A multiplexer (MUX) consists of many data input lines and only one output line. In Fig. 4, a 4 transistor 2:1 MUX chooses an output from different inputs based on the select signal. [7].

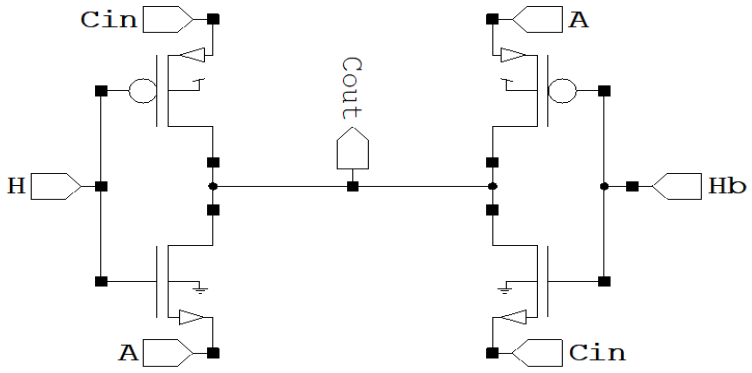


Fig.4: Shows Schematic View onEDA Tool Full-Swing GDI 2*1 Multiplexer

D. Design of Full Adder

When in combinational circuit three inputs are given and arithmetic operation is performed by that combination circuit that is called FA [8]. Addition is recognised as a fundamental operation in both arithmetic as well as digital signal processing. The one-bit FAconsists two output bits: carry out, and sum, which represents the result of the addition operation. The operandsare bits A and B. Cin is the third input bit that was carried over from the less important stage before.

The optimized design, is shown in fig. 6, Ten transistors make up the block diagram in fig.5 and the truth table for the optimised complete adder in Table III, including two XOR gate cells for sum and one MUX cell for carryout.

Table 3: Truth Table of optimized FA

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	0	0	1	0
0	0	1	0	1
1	1	0	1	0
1	1	1	0	1
1	1	0	0	1
1	1	1	1	1

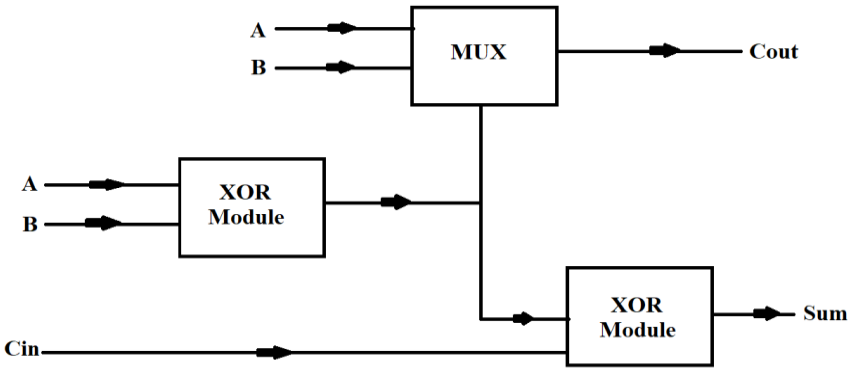


Fig.5: Block Diagram of Optimized GDI based Full Adder Design

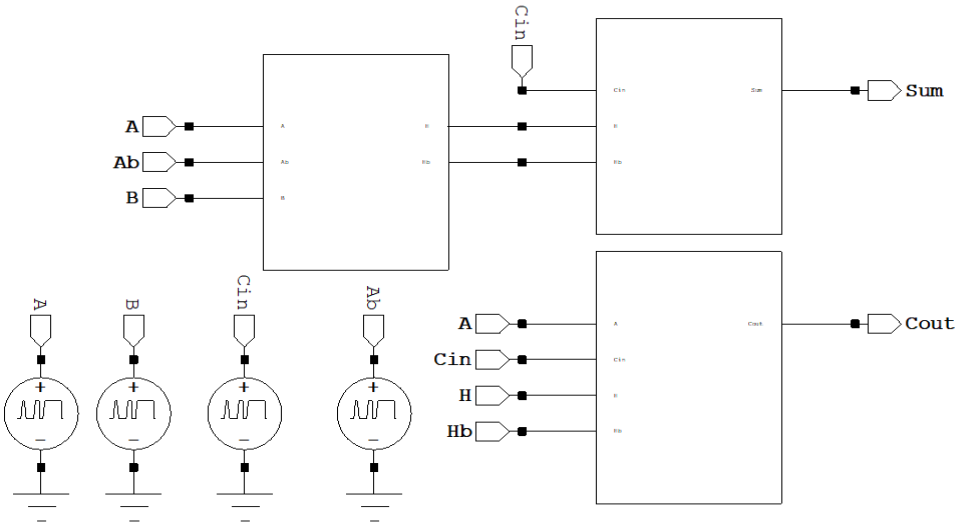


Fig.6: Schematic View on EDA Tool for OptimizedFA

5. APPLICATIONS OF THE PROPOSED DESIGN OF FA

A. ARITHMETIC LOGIC UNIT(ALU)

ALU is a component of the central processor unit that performs arithmetic and logical operations. Fig. 8 shows Block Diagram of ALU. The speed of the arithmetic unit is critical, as it is heavily influenced by the multiplier's speed. As a result, technology is constantly exploring for new algorithms and hardware to accomplish this function in a much more space and time efficient manner. Vedic Mathematics includes arithmetic, algebra, geometry, and other fields of mathematics. The incorporation of Vedic Mathematics concepts in a processor's processing method reduces the complexity of the execution time, area, and power consumption, among other things. The UrdhavTriyagbhyam Vedic method for multiplication differs from the actual multiplication process by allowing parallel synthesis of transitional products, removing needless steps of multiplication along with zeros, and scaling to bits of higher levels. This formula (Sutra) can be used to create a processor with a high speed, energy-efficient multiplier. This project intends to increase the performance of an ALU by designing an arithmetic and logic unit utilising old Indian Vedic Mathematics techniques.

ALU performs multiplication, division, addition and subtraction. To perform the multiplication operation Vedic multiplier is used and for addition proposed full adder of 10T hybrid logic is used.

B. RIPPLE CARRY ADDER FOR VEDIC MULTIPLIER IMPLEMENTATION

In Ripple Carry Adder, full adders are configured in a format to produce the result of adding a bit-n-bit string. Fig.7 shows Four-bit Ripple Carry Adder(RCA).

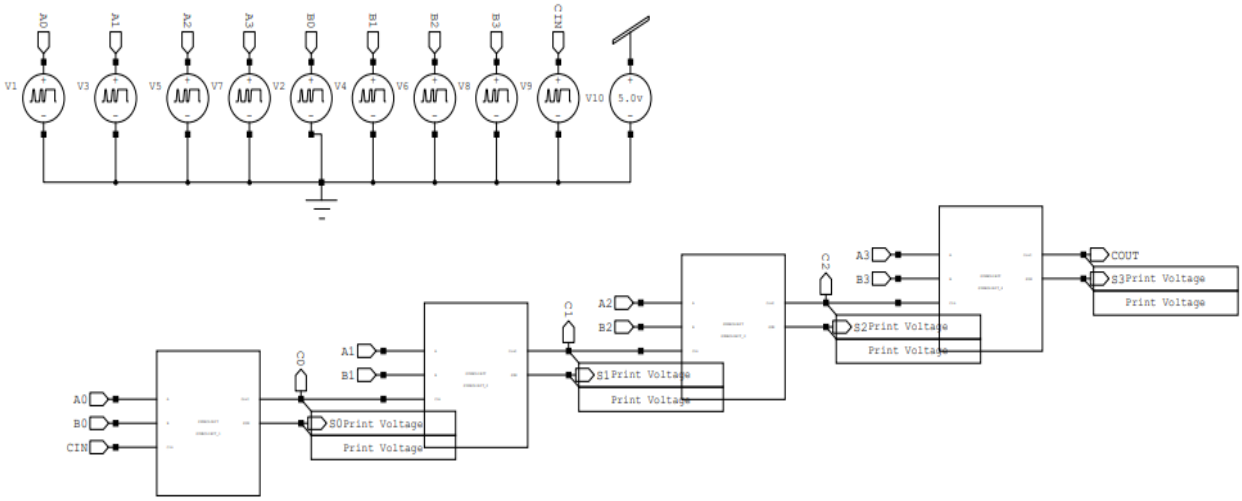


Fig 7: Ripple carry adder with four-bit output

6. RESULTS & COMPARATIVE ANAYLSIS

The optimized Full Adder circuit design of one bit is created using TSMC's 65nm technology. Simulations were performed using the EDA TOOL with a power supply of 0.8 V and transistor sizes of $W_p/L=260/65$ for PMOS and $W_n/L=130/65$ for NMOS to obtain the best power and delay presentation. The suggested Full Adder's waveform is illustrated in Fig. 9, and Table IV compares its performance to that of the devices in References [1], [2], [8], [9] and [10]. The suggested design for a 1-bit FA uses less power than earlier iterations since it uses less transistors to form circuits, offers less latency and has a full-swing output.

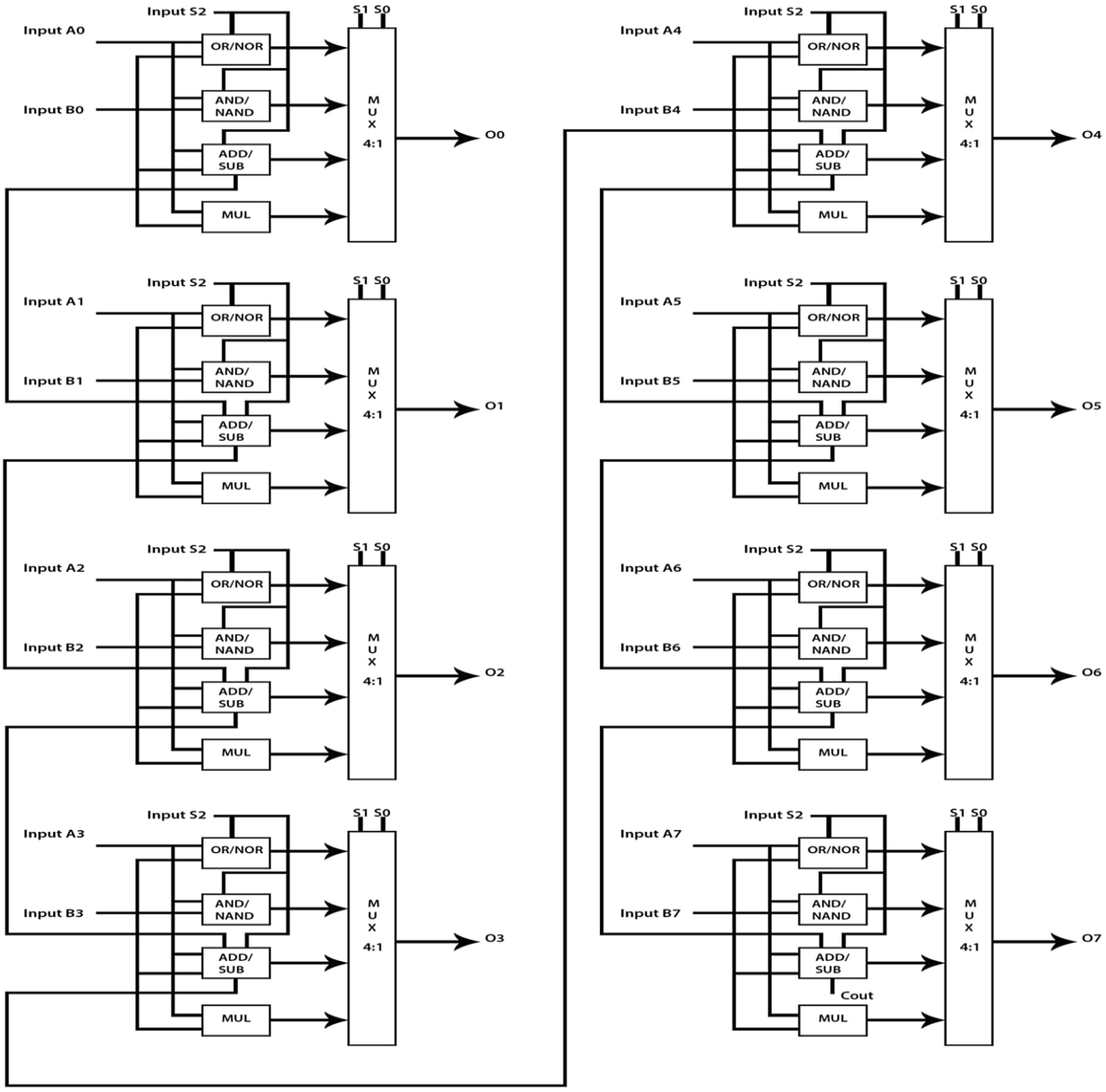


Fig. 8: Block Diagram of Arithmetic Logic Unit

Table4: Comparative results of Optimized GDI based Full Adder Design on 65nm

Design	No. of trans.	Power (nW)	Delay (ps)	Vdd	Tech (nm)
18T Hybrid Full Adder [1]	18	3770	229.8	1.8	180
Full Adder using GDI Technique[2]	16	693.5	2.5	2.5	65
Low power CLA design [8]	18	927.9	37.86	1.1	45
Efficient 1-bit Full Adder [9]	10	8100	6.47	Nil	45
GDA based full adder design [10]	21	9000	18	1.2	120
OptimizedGDI based Full Adder Design on 65nm	10	674.38	2.3	0.8	65

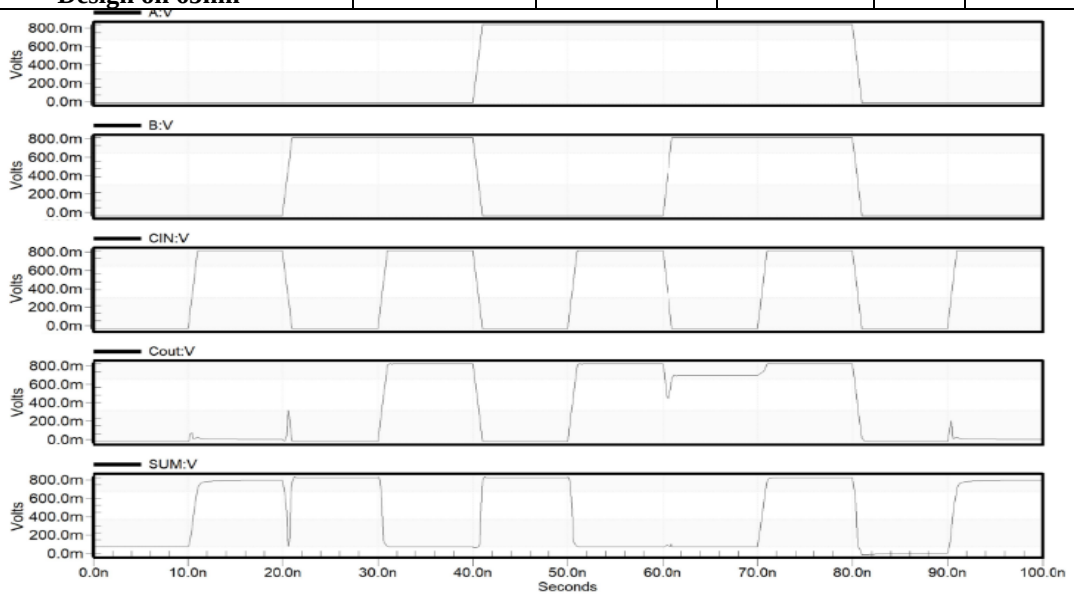


Fig.9: Output of optimized 10T Hybrid Full Adder using 65nm technology

7. CONCLUSION

This paper demonstrates a 1-bit FA that was created using the GDI approach in 65nm Technology and was simulated on EDA Tool. The results of the simulation demonstrated how to retain full swing operation while reducing transistor count,propagation delay and power consumption. Ten transistors make up the suggested design, which runs on a 0.8 supply voltage. This study compares and contrasts the present design with the FA's suggested work in respect of power and delay.This design is low power and area efficient FA consumes 82% less power and delay is 99% less than existing 18 hybrid full adder design [1] and also consumes 92% less power and delays 87% less than GDI based exiting design of FA [10]. The proposed Optimized FA can be used in the Ripple Carry adder shown in Fig. 7 that is ultimately used in ALU shown in Fig. 8 above to improve to performance.

8. FUTURE SCOPE

A key component in the data stream of many microprocessor- and microcontroller-based systems is the Full Adder (FA). The entire design intended for an application will also be optimised as a result of additional optimization of this essential unit in aspect of power and delay of operation of Full Adder.

Data availability: This article does not qualify as data sharing because no datasets were created or analyzed for the current research.

Conflict of Interest: There are no conflict of interests.

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