Design and Analysis of MOS only Active Inductor Circuit and its 2nd Order Band Pass Filter application

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Abstract

This paper presents active inductor circuit designed with only MOS. The circuit have four MOS transistors only and no additional biasing current sources. The proposed design of active inductor offers small chip area, tunability and low power consumption of 172 µW. To analyse the performance of active inductor, a 2nd order bandpassfilter structure is demonstrated with low noise as 7.16nV/√Hz. Contrary to the latest State of Art, the proposed design of Active Inductor is an all MOS inductor with no passive components and current sources incorporated in the device. Cadence Virtuoso is used to simulate proposed active inductor and filter using a 90nm CMOS technology.

Keywords: Active Inductor;MOS transistor; Inductance; Simulator; Analog filters; Analog Integrated Circuit.

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1. INTRODUCTION

In RF systems, passive inductors are used in a variety of applications, including filters, oscillators, biasing, phase shifters, etc. They do, however, have significant drawbacks, such as taking up more chip space, a lower quality factor, and higher inductance value. As a result, in many applications, active inductors made with MOS transistors are preferable. CMOS active inductors has advantages over passive spiral inductors, including tunability, a high quality factor, a big inductance value, low noise, a small chip area, and low power consumption.[2]Active elements are used in a number of active inductor circuits, including the operational trans-resistance amplifier (OTRA)[7], dual X 2nd generation current conveyor (DXCCII)[5-6], voltage differencing buffered amplifier (VDBA)[3], and voltage differencing current conveyor (VDCC)[4], a current conveyor of the first generation (CCI)[8], the current feedback operational amplifier (CFOA)[9-11]. In the literature, differential difference current conveyor (DDCC)[13] and current differencing transconductance amplifier (CDTA)[12] have both been documented. Active inductors using MOS transistors and passive components[17–18] as well as MOS-only active inductors[14–16] have both been developed. The literature has, however, used active filter circuits that use solely MOS[21-25].

In [1], the authors describe MOS only designs of active inductor circuits. Each circuit employs two MOS transistors along with two biasing currents. With150 µW and 90 µW of power consumption respectively, the suggested active inductors offer tunability, low power consumption and small chip area. A 2nd order band-pass filter and a 3rd order high-pass filter is demonstrated with low noise in order to examine their performance. LTSPICE is used to simulate the active inductors and filters in 180nm CMOS process.

This paper's primary goal is to demonstrate a MOS-only active inductor circuit that uses the fewest possible transistors. It offer stunability, low power consumption and small chip area. The qualitative and quantitative performance of suggested active inductor is contrasted with findings in the literature[1, 3–9,12,13,17,18] in Table 1. Cadence Virtuoso is used to simulate proposed active inductor using a 90nm CMOS technology. Additionally, a 2nd order bandpass filter is designed to demonstrate the adaptability of using the proposed design of active inductor. The structure of this paper is: The proposed design of the active inductor is presented in Section 2, along with its qualitative merit and comparison. This research addresses the challenge of reducing chip area, power consumption, and dependency on passive components in active inductor circuits, which are essential for RF applications. Current designs with passive

components or biasing currents often lack the flexibility and compactness needed for efficient integration. Our design focuses on a MOS-only configuration, optimizing for tunability and minimal component use without additional current sources. This approach aims to achieve a balance of high performance and compact design, demonstrated through a 2nd order band-pass filter application. In Section 3, the Filter application of proposed design is covered. The results and simulation findings of filter application are in Section 4. Then, the study is concluded in Section 5.

2. PROPOSED DESIGN

The inductance of a passive inductor depends on the permeability (μ) of material the core material, no. of turns in the coil(N), area of cross section(A) and length of the coil(l)is given by:

$$\mathbf{L = (\mu N^2 A)/l}$$

For a passive inductor having coil with specific physical properties, the inductance value is fix and cannot be varied. However, active inductor is a coil(or inductor) less circuit and the inductance can varied by varying different parameters in the circuit. An active inductor[1] is shown in Figure 1, which is based on gyrator-C circuit topology shown in Figure 2(a), in which G_{m1}, G_{m2} are transconductances, Go1 and C1, Go2 and C2 indicate the total conductances and capacitances respectively. Gyrator based design of active inductor occupies small chip area and offers better linearity.

Figure 2(b) provides the equivalent passive circuit of active inductor. I/p admittance of the active inductor shown in Figure 1, can be evaluated as:

$$Y= [I_{in}/V_{in}] = g_{o1} + g_{o2} +g_{m1} + s*C_{gs1} + [(g_{o1} + g_{m1})* (g_{m2} – g_{o1})]/[(g_{o1} + s*C_{gs2})] \quad (1)$$

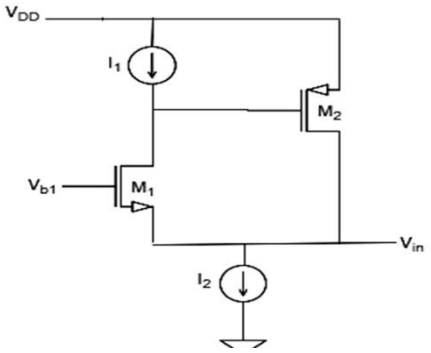
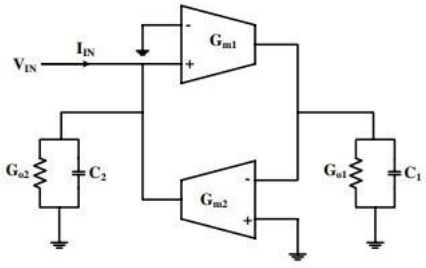


Figure1: Active Inductor Circuit



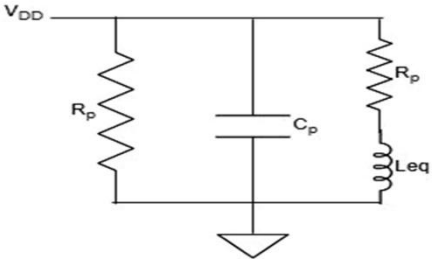


Figure 2(a): Gyrator-C circuit topology Figure 2(b):Passive Equivalent circuit of active inductor

Analysing Eq. (1) gives,

$$R_p = 1/[g_{o1} + g_{o1} + g_{m1}],$$

$$C_p = C_{gs1},$$

$$R_s = g_{o1}/[g_{m1}*g_{m2}],$$

$$\mathbf{L_{eq} = C_{gs2}/[g_{m1} * g_{m2}]} \quad \mathbf{(2)}$$

where C_{gsi}represents gate to source capacitance; g_{oi}representsg_{dsi} of transistor Mi.

The structure in Figure1 is super source follower (SSF) based circuit. SSF circuit is an increased swing modification of flipped voltage follower (FVF). As a result, the FVF's problem with a tiny voltage swing is solved. Better current efficiency, lower output impedance, reduced distortion and then FVF[20] are some additional benefits of SSF.

The schematic design of proposed active inductor designed on Cadence Virtuoso is shown in Figure 3. In the proposed design of active inductor, the two biasing currents I_1& I_2 shown in Figure-1 has been replaced with PMOS & NMOS in saturation region which are working as current sources and hence the requirement of biasing currents is eliminated. The proposed active inductor is designed using CG (Common Gate) and CS (Common Source) stages. Figure 3, the transistor with positive transconductance is designed as a CG, and the transistor with negative transconductance is configured as a CS. CG-CS configuration offers benefits such as low power, low supply voltage designs.[8]

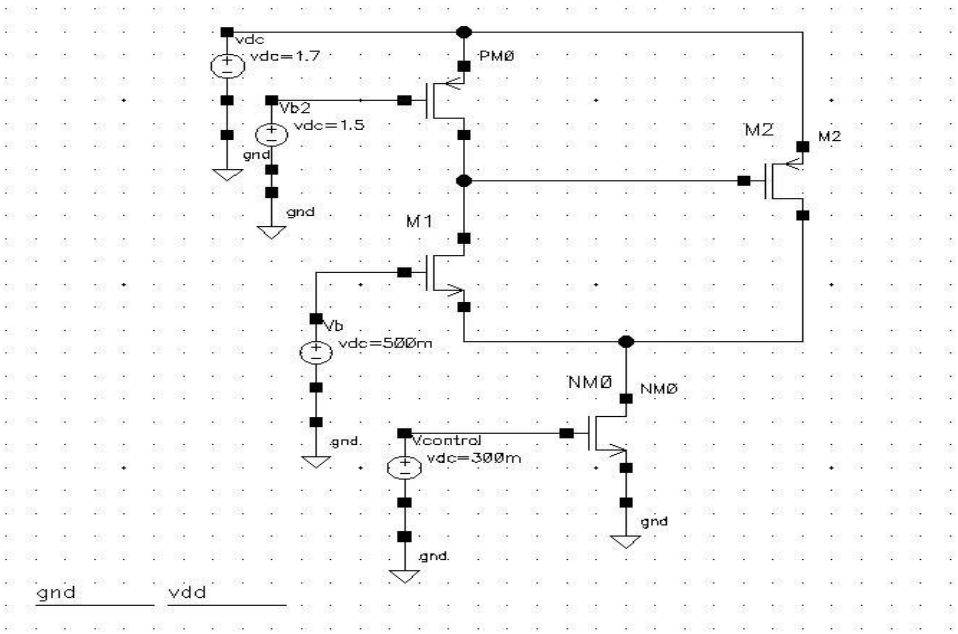


Figure 3:Active inductor circuit design proposed

The proposed design of active inductor given in Figure 3 is simulated with Cadence Virtuoso 90nm CMOS process model parameters. The supply voltage is kept as VDD = 1.7v and the Vb1 provides DC voltage bias for M2 at 0.5v. The transistors used in the proposed active inductor have dimensions: W1 = W2 = 14.4 µm and L1 = L2 = 0.36 µm. NM0 & PM0 acts as current sources by operating them in saturation region.

The proposed design offers tunability as the value of inductance can be modified by varying g_m values through Control Voltage (Vcontrol) applied to transistor NM0as shown in Figure3. Inductance values of the proposed design for different control voltages from 300mV to 400mV applied at NM0 obtained through Cadence Virtuoso tool are shown in Table-2&Figure 4.As the control voltage increases from 300mV to 400mV, the inductance value decreases. The peak power consumption of this active inductor circuit is 172.76 µW and is shown in Figure 5. There is qualitative improvement in the design as there are just four MOS transistors in the circuit and no additional active or passive component are used.To realize the proposed MOS-only active inductor practically, several critical parameters were carefully optimized. The transconductance (Gm) and gate-source capacitance (Cgs) of the MOS transistors were adjusted to achieve the required inductance values effectively. The design incorporates common gate (CG) and common source (CS) stages, which enhance both stability and tunability. This configuration allows the circuit to respond flexibly to variations in the control voltage, enabling adjustments to the inductance levels as needed.

In place of traditional biasing currents, the design utilizes PMOS and NMOS transistors operating in the saturation region as current sources, which effectively reduces the overall power consumption without sacrificing performance. This innovative approach, free from passive components and extra current sources, provides a practical model for real-world applications, particularly in RF circuits where low power and compact chip area are essential. As a result, the proposed model demonstrates feasibility and efficiency for applications in RF filtering, oscillators, and other compact analog circuits.

Table-2: Equivalent inductance of proposed active inductor for Control Voltages (Vcontrol)

Vdd	Cgs2 (f)	gm1 (u)	gm2 (u)	Leq(nH)	Vcontrol (mV)
1.7	72.467	241.135	912.13	329.4756256	300
1.7	72.953	244.994	1037.23	287.0864123	320
1.7	73.213	248.441	1155.58	255.0145251	340
1.7	73.328	251.541	1267.77	229.9432081	360
1.7	73.353	254.342	1374.09	209.886555	380
1.7	73.321	256.884	1475.14	193.4898041	400

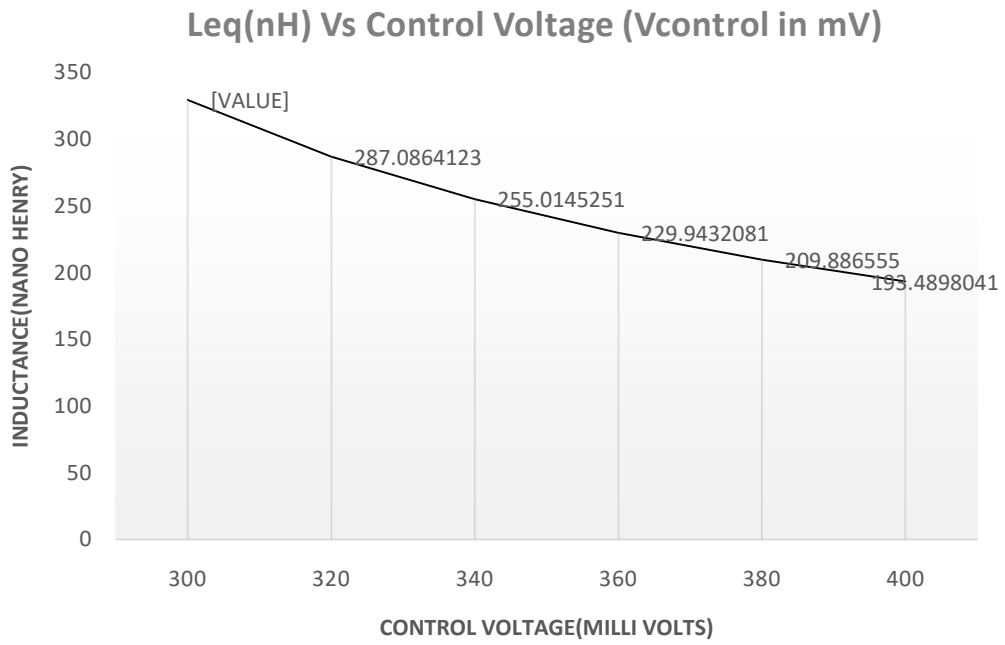


Figure 4:Variation of Inductance values of proposed design of active inductor at different Control Voltages

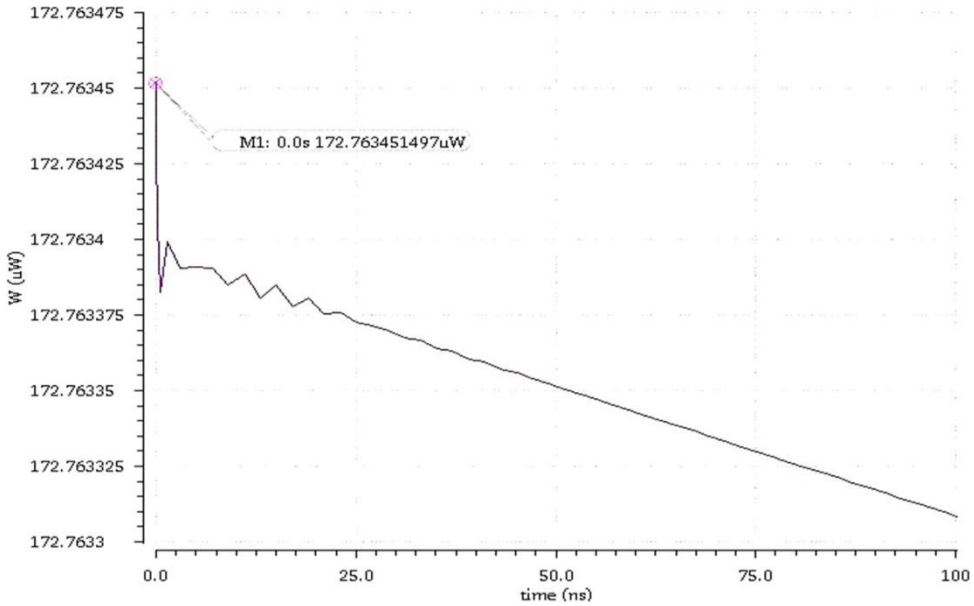


Figure 5. Power Consumption value of proposed active inductor for $V_{control}$ = 300mV.

Table-1: Comparison of performances of different active inductor designs

Reference Design	Number of transistor	Current Sources / Passive elements	Tunability	Power Consumptions (µW)	Technology (nm)	Supply Voltage (V)
Proposed Active Inductor	4	No active & passive elements are used	YES	172	@90	1.7
[1]	2	Two Biasing Current Sources are used	YES	150	@180	1.5
[3]	_	VDBA:1 / 1R, 1C	YES	_	_	_
[4]	22	VDCC: 2 / 1R, 1C	YES	869	_	1.8
[5]	48	DXCCII:1 / 2R, 1C	_	_	@350	3
[6]	29	DXCCII:1 / 2R, 1C	YES	_	@350	3.3
[7]	14	OTRA:1 / 3R, 2C	YES	809	_	3
[8]	26	CCI:1 / 4R, 1C	_	985	_	3.3
[9]	_	CFOA:1 / 2R, 1C	_	_	_	_
[12]	_	CDTA:2 / 1C	_	_	_	5
[13]	18	MDO-DDCC:1 / 2R,1C	_	_	@350	3
[17]	3	_ / 1R, 1C	YES	515	@90	1
[18]	6	_ / 1C	_	1000	@130	1.2

The proposed MOS-only active inductor offers several advantages over conventional designs, making it particularly suitable for RF applications. Unlike designs that rely on passive components or additional biasing currents, our model eliminates the need for these components, which significantly reduces chip area and power consumption. By using a configuration with just four MOS transistors, the design minimizes complexity while maintaining high tunability, allowing the inductance to be adjusted via control voltage. This compact and energy-efficient structure contrasts with other designs that require a larger number of transistors or rely on external current sources, leading to higher power requirements. Additionally, our solution demonstrates low noise levels, an essential factor for RF circuits where signal integrity is crucial. These improvements—small chip area, low power consumption, and high tunability—highlight the practical advantages of our MOS-only design over alternative approaches.

3. FILTER APPLICATION DESIGNED USING PROPOSED DESIGN OF ACTIVE INDUCTOR

A Band Pass(BP) allows signal with certain range of frequencies (called pass band) to pass through it and attenuates the signal out of this range of frequency. A BP filter is designed by cascading a High pass filter and a low pass filter stages. The pass band of a band pass filter designed by cascading a high pass filter having lower cut-off frequency f_L and a low pass filter having higher cut-off frequency f_H is shown in Figure 6(a) below:

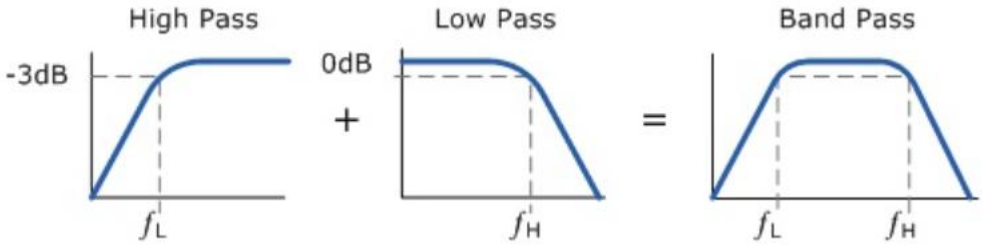


Figure 6(a): Pass band of BP Filter

To demonstrate the effectiveness of proposed design of active inductor(Figure3), a 2nd order bandpass filter shown in Figure6(b) is designed. The 2nd Order BP Filter is simulated on Cadence Virtuoso at 90nm technology and is shown in Figure 6(c).

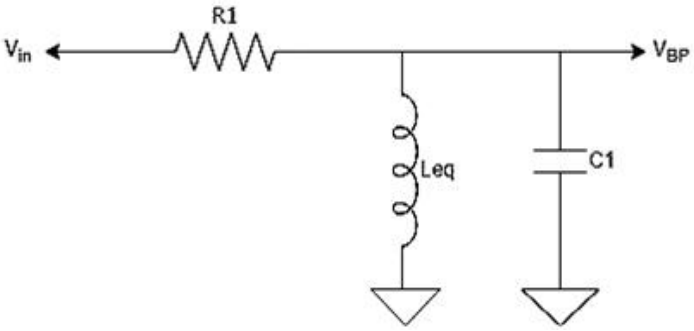


Figure6(b): 2nd Order BPFilter structure

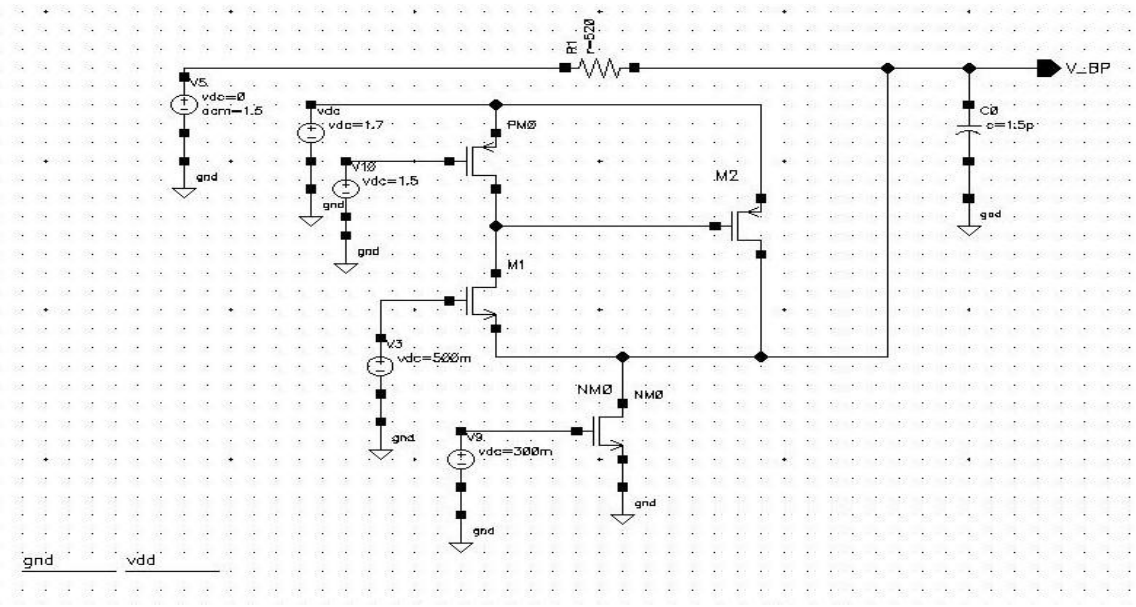


Figure6(c): 2nd Order BP Filter designed with the proposed design of active inductor

4. RESULTS

To design the 2nd Order Band Pass Filter given in Figure6(c), the value of the passive components are selected as: R_1 = 520, C_1 = 1.5 pF and L_{eq1} = 329.47nH (value of inductance of proposed design given in Figure3). The 2nd order BP filter structure given in Figure 6(c) is simulated and its frequency responses are shown in Figure 7(a), (b) and (c). The Bandwidth of the BP Filter is 293.13 MHz [512.54 – 219.412 MHzi.e. the difference between upper cut-off(f_H) and lower cut-off(f_L) frequencies] as shown in Figure 7(a).The phase of the filter varies from 34.28 deg. to -49.35 deg. in the pass band extending from 219.412 MHz to 512.54 MHz. The variation of phase with frequency of operation is shown in Figure 7(b).The noise varies from 15.32 nV/√Hz to 7.16 nV/√Hz in the pass band. Further, the noise at centre frequency 338.3 MHz is 14.4 nV/√Hz. The minimum noise offered by the 2nd Order Band Pass Filter in the pass band is 7.16 nV/√Hzat 512.544 MHz as shown in Figure7(c).

The pass band of the 2nd Order Band Pass Filter can be shifted by varying the inductance through Control Voltage applied at NM0 shown in Figure 6(c).

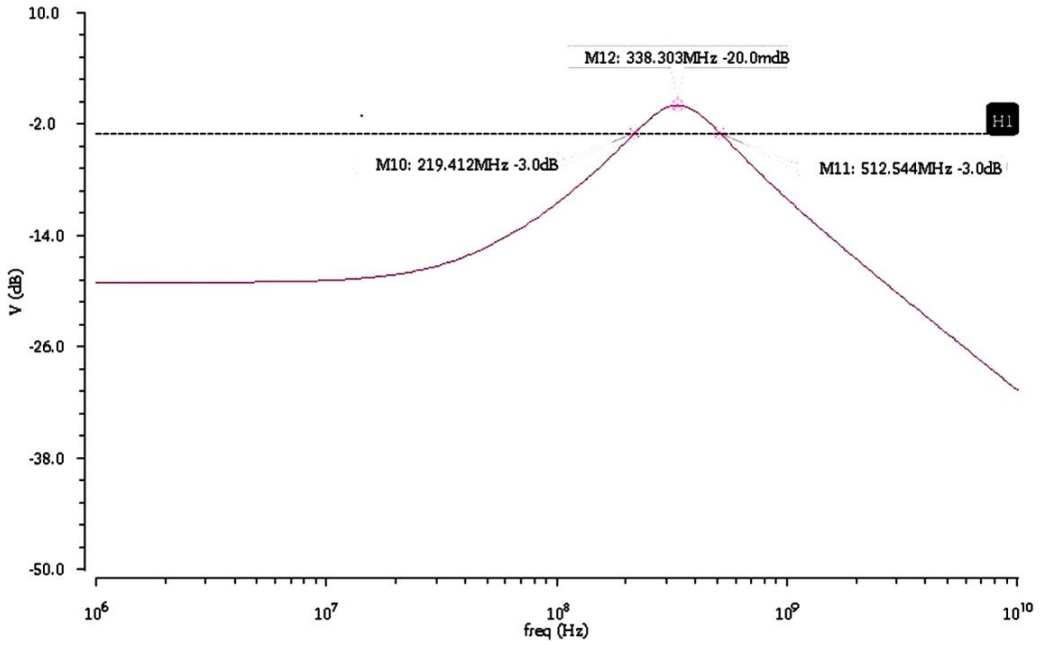


Figure7(a): Gain(20 dB) Vs Frequency Plot of 2nd Order BP Filter

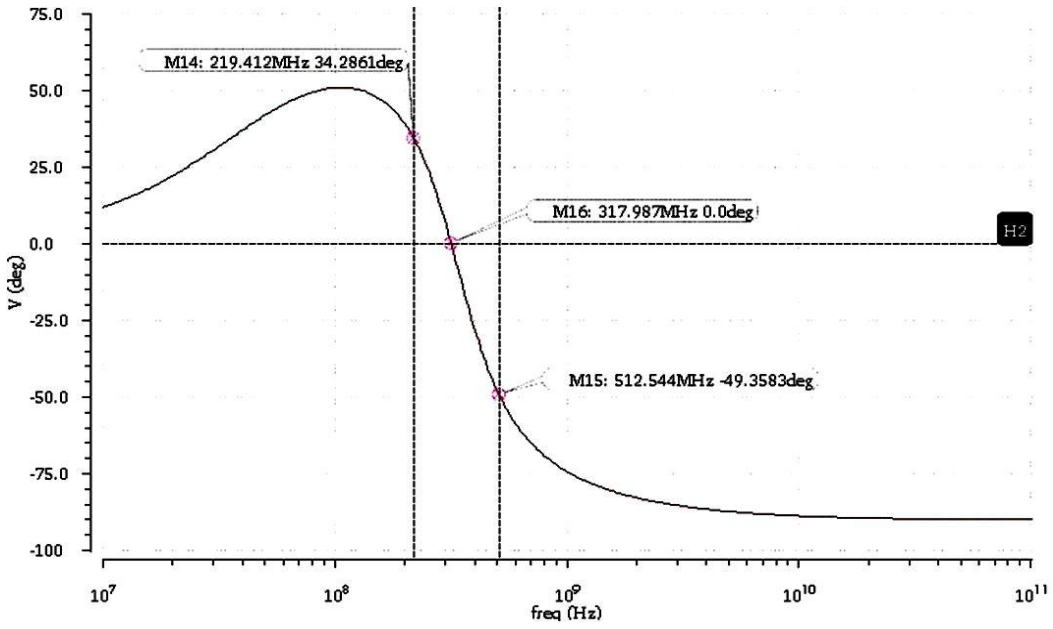


Figure7 (b): Phase Vs Frequency Plot of 2nd Order BP Filter

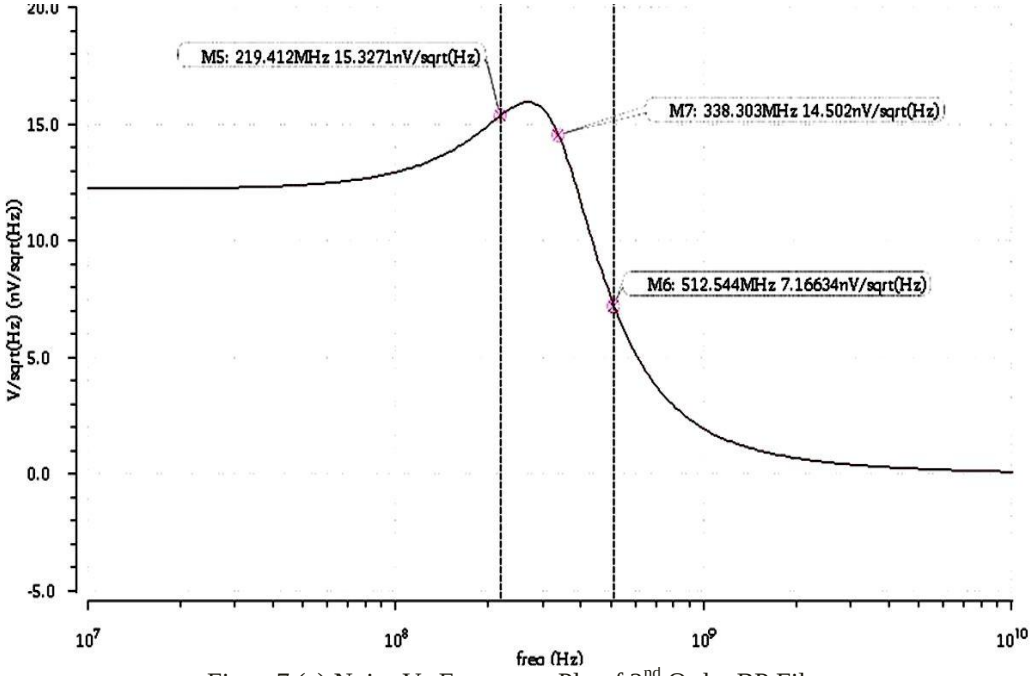


Figure7 (c):Noise Vs Frequency Plotof 2nd Order BP Filter

The above application proves that the proposed MOS-only active inductor design demonstrates significant advancements in RF circuit technology by achieving a high level of performance with minimal components. The design successfully eliminates the need for passive components and additional biasing currents, resulting in a compact circuit with reduced chip area and lower power consumption. These results validate the design's practicality and efficiency, marking it as an adaptable solution for RF applications requiring small form factors and energy-efficient operation. By integrating tunability through control voltage adjustments, this design offers a practical alternative that sets a new benchmark in active inductor performance. This work establishes a new standard in active inductor design, addressing current limitations and offering a practical solution that combines simplicity with high performance, positioning it as a valuable contribution to modern RF applications.

5. CONCLUSION

An active inductor circuit using only MOS is demonstrated in this paper. There are just four MOS transistors in the circuit and no additional active or passive component are used. The circuit offers tunability, area reduction, low noise, low power supply. Also, there is qualitative improvement in the design as there are just four MOS transistors in the circuit and no additional current sources or passive components are used. A 2 nd order BP filter has been designed to test, if employing proposed design of active inductors in RF filters is feasible. The Band Pass Filter's bandwidth is of 293 MHz and offers low noise of 7.16 nV/√Hz at 512.544 MHz. Using 90nm CMOS technology, Cadence Virtuoso is used to simulate the circuits. The proposed implementation can be utilized to design electronically tunable large value of inductance needed to design integrated circuit active filters and other analog circuits like tuning circuits, induction motors, sensors, power divider, power combiner, matching circuits etc.

6. FUTURE SCOPE

A key component for designing integrated circuit active filters, transmitters, receivers are the Active Inductors. The entire design intended for an application will also be optimised, as a result of additional optimization of this essential unit in aspect of tunability, power, chip area and bandwidth further improvement in operation of Active Inductor will be done.

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